



# Richard C. Walker

Agilent Technologies · Mass Spectrometer Division

10.96 · MSCS BSEE

About Current research Research

## About

Introduction

### Current Institution

**Agilent Technologies**  
Mass Spectrometer Division  
Santa Clara, California

Current position

Senior R&D Electrical Engineer

### Skills and Expertise

- Electronics
- Analog Electronics
- Circuit Simulation
- Circuit Analysis
- Spice Simulation
- Microprocessor Programming
- Embedded Systems Programming
- Analog Signal Processing
- Electronic Amplifiers
- Integrated Circuits
- Electronics and Communication
- Analog Circuits
- PLL
- PIC
- Analog IC Design
- Phase Locked Loop



Richard Walker was born in San Rafael CA, in 1960. He received the B.S. degree in Engineering and Applied Science from the California Institute of Technology in 1982, and an M.S. degree in Computer Science from California State University, Chico, CA in 1992. Rick joined Agilent Laboratories (formerly Hewlett-Packard Laboratories) in 1981, where he is currently a Principal Project Engineer. Since that time, he has worked in the areas of broadband-cable modem design, solid-state laser characterization, phase-locked-loop theory, linecode design, and gigabit-rate serial data transmission. He holds 15 U.S. patents.

Richard C. Walker. (Feb.2001). Designing Bang-Bang PLLs for Clock and Data Recovery in Serial Data Transmission Systems. Hewlett-Packard.

52  
Research items  
485  
Reads  
298  
Citations

### Research Experience

Jan 1981 - Jan 2002

**Principal Staff Scientist**  
Hewlett-Packard  
Palo Alto, United States

Top co-authors

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**Barclav Tullis**



Novelthink



**Jeffrey King**  
Corning Incorporated



**C.-S. Yen**  
Not yet on ResearchGate

✓ Invited



**C. Stout**  
Not yet on ResearchGate

✓ Invited



**B. Lai**  
Not yet on ResearchGate

✓ Invited

Followers

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Following



Current research

Projects (1)

**10G ethernet**

Archived project

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## Research

Research Items

**Optical Engines and Optical-Cable Assemblies Capable of Low-Speed And High-Speed Optical Communication**Patent [Full-text available](#) Dec 2015

Mathieu Charbonneau-Lefort · William Richard Trutna · Richard C. Walker · Michael John Yadlowski

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**Optical Touch - Screen Systems And Methods Using A Planar Transparent Sheet**Patent [Full-text available](#) Dec 2015

Jeffrey King · Timothy James Orsley · William Richard Trutna · Richard C. Walker

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**Robust Optical Touch - Screen Systems And Methods Using A Planar Transparent Sheet**Patent [Full-text available](#) Jun 2015

Jeffrey King · Dragan Pikula · Richard C. Walker

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**Integrated circuit for facilitating optical communication between electronic devices**Patent [Full-text available](#) Sep 2014

Richard C. Walker

Active optical cable assemblies, and systems, methods, and adapter modules and integrated circuits for facilitating communication between a host and a client device over a fiber optic cable are disclosed. In one embodiment, an active optical cable assembly includes a fiber optic cable having at least one optical fiber, a host active circuit, a client active circuit, a host connector, and a client connector. Upon a connection between...

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**Integrated circuit for facilitating optical communication between electronic devices**Patent [Full-text available](#) Sep 2014

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**Apparatuses, systems, and methods for facilitating optical communication between electronic devices**Patent [Full-text available](#) Mar 2013

Richard C. Walker

Active optical cable assemblies, and systems, methods, and adapter modules and integrated circuits for facilitating communication between a host and a client device over a fiber optic cable are disclosed. In one embodiment, an active optical cable assembly includes a fiber optic cable having at least one optical fiber, a host active circuit, a client active circuit, a host connector, and a client connector. Upon a connection between...

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**Multi-phase sampling**Patent [Full-text available](#) May 2007

Richard C. Walker

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**Coding method for coding packetized serial data with low overhead**Patent [Full-text available](#) May 2006

Richard C. Walker · Birdy Amrutur · Richard Dugan

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**Immersive Display System**Patent [Full-text available](#) Mar 2005

Richard C. Walker · Pierre Mertz · Barclay Tullis

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### Data communication system with self-test facility

Patent [Full-text available](#) Mar 2005

Richard C. Walker · Patricia A. Thaler

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### Network monitoring system with built-in monitoring data gathering

Patent [Full-text available](#) Jan 2005

Richard C. Walker · Bharadwaj Amrutur · Peter Mottishaw · [...] · Ian Hardcastle

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### Electro-optical material-based grey scale generating method

Patent [Full-text available](#) Sep 2004

Richard C. Walker · Travis N. Blalock · Neela B. Gaddis

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### Multiplexer with channel sectioning, selectively actuated current sources, and common-base amplifiers

Patent [Full-text available](#) Jul 2004

Peter Ho · Graham M. Flower · Richard C. Walker

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### Adaptive decoder for skin effect limited signals

Patent [Full-text available](#) Jul 2004

Adrian Wan-Chew Seet · Ken Nishimura · Richard C. Walker

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### Personal viewing device with system for providing identification information to a connected system

Patent [Full-text available](#) May 2004

Rene Helbing · Richard C. Walker · Pierre Mertz · [...] · Ken A. Nishimura

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### Coding method and coder for packetized serial data with low overhead

Patent [Full-text available](#) Apr 2004

Richard C. Walker · Birdy Amrutur · Richard Dugan

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### Decoding method and decoder for 64b/66b coded packetized serial data

Patent [Full-text available](#) Nov 2003

Richard C. Walker · Birdy Amrutur · Richard Dugan

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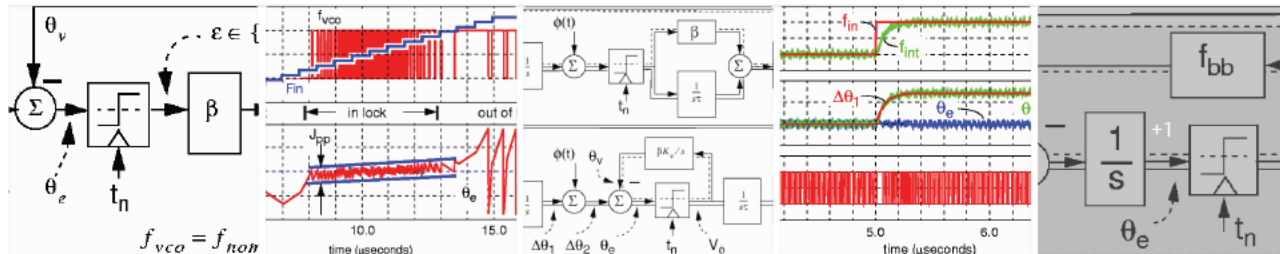
### Immersive Display System

Patent [Full-text available](#) Apr 2003

Richard C. Walker

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### Designing Bang-Bang PLLs for Clock and Data Recovery in Serial Data Transmission Systems

Chapter [Full-text available](#) Jan 2003 · "Phase-Locking in High-Performance Systems - From Devices to Architectures"

Richard C. Walker

Clock recovery using phase-locked loops (PLL) with binary (bang-bang) or ternary-quantized phase detectors has become increasingly common starting with the advent of fully monolithic clock and data recovery (CDR) Circuits in the late 1980's. Bang-bang CDR circuits have the unique advantages of inherent sampling phase alignment, adaptability to multi-phase sampling structures, and operation at the highest speed at which...

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System and method for encoding an input data stream by utilizing a predictive, look-ahead feature. United States

System and method for encoding an input data stream by utilizing a predictive, look-ahead feature, United States

Patent Full-text available Dec 2002

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Method and system for compensating for defects in a multi-light valve display system

Patent Full-text available Mar 2002

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Electro-optic material based display device having analog pixel drivers

Patent Full-text available Dec 2001

Richard C. Walker · Travis N. Blalock · Neela B. Gaddis

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64b/66b decoding for packetized serial data

Patent Full-text available Sep 2001

Richard C. Walker · Birdy Amrutur · Richard Dugan

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Coding for packetized serial data

Patent Full-text available Sep 2001

Richard C. Walker · Birdy Amrutur · Richard Dugan

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Analog pixel drive circuit for an electro-optical material-based display device

Patent Full-text available Jun 2001

Travis N. Blalock · Neela B. Gaddis · Richard C. Walker

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Oversampling Rotational Frequency Detector

Patent Full-text available Apr 2000

Bin Wu · Richard C. Walker

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Fully Integrated High-Speed Interleaved Voltage-Controlled Ring Oscillator

Patent Full-text available Nov 1998

Tom Knotts · C. Stout · Richard C. Walker

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Modulation and Frequency Conversion by Time Sharing

Patent Full-text available Oct 1997

Hornak · A. Z. Grzegorek · W. McFarland · [...] · S. D. Wil ingham

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A 2.488 Gb/s Si-bipolar clock and data recovery IC with robust loss of signal detection

Conference Paper Full-text available

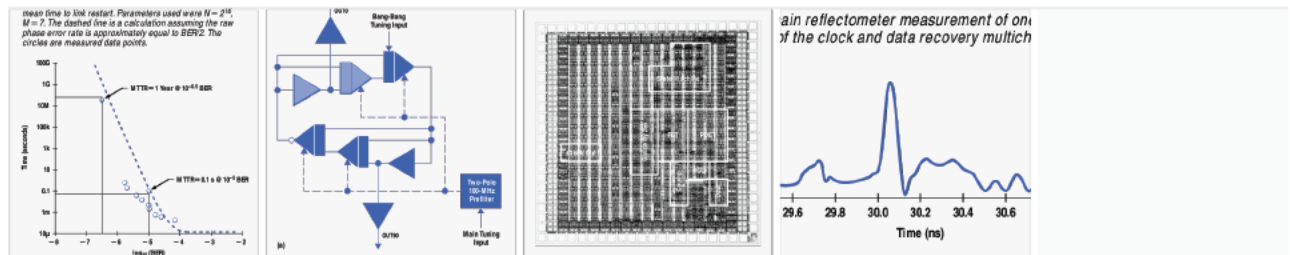
Mar 1997 · Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International

Richard C. Walker · C. Stout · C.-S. Yen

SONET 2.488Gb/s transmission and switching systems, network backbones, and video transmission are among the many application areas benefiting from inexpensive and robust clock and data recovery circuits (CDR). Previous commercial solutions have required multiple chips and GaAs processes to perform this function. This 25GHz Si-bipolar chip operates from 2 to 3Gb/s over worst-case process,...

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A 2.488-Gbit/s silicon bipolar clock and data recovery circuit for SONET fiber-optic communications networks

Article Full-text available Jan 1997 · Hewlett-Packard Journal

Richard C. Walker · C. Stout · C.-S. Yen · L.R. Dove

Adjustment-free clock and data recovery for 2.488-Gbit/s SONET applications is provided by a 1.77W, 3.45 × 3.45-mm<sup>2</sup> chip implemented in a 25-GHz ft silicon bipolar process. The chip has an on-chip VCO and operates from 2 to 3 Gbits/s over process, voltage, and temperature variations with a single off-chip filter capacitor. For network monitoring, a highly reliable loss-of-signal detector is provided. For good mechanical, thermal,...

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#### Unity Gain Positive Feedback Integrator with Programmable Charging Currents

Patent Full-text available Mar 1996

B. Lai · Richard C. Walker

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#### DC- Free Line Code for Arbitrary Data Transmission

Patent Full-text available Aug 1995

Crandall · S. R. Hessel · T. Hornak · [...] · Richard C. Walker

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#### INTRODUCTION TO THE SPECIAL ISSUE

Article Dec 1994 · IEEE Journal of Solid-State Circuits

IA YOUNG · SS TAYLOR · Richard C. Walker

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#### A general-purpose link interface chipset for gigabit rate datacommunication

Conference Paper Full-text available

Jan 1993 · Global Telecommunications Conference, 1992. Conference Record., GLOBECOM '92. Communication for Global Users., IEEE

C.-S. Yen · Richard C. Walker · C. Stout · [...] · J. Win

A chipset has been developed for transmitting parallel data over serial links. The chipset, consisting of a transmitter interface chip (TIC) and a receiver interface chip (RIC), can support serial transmission up to 1.4 Gbaud. Data encoding is based on a scheme published earlier, but has been improved to provide more flexibility and better efficiency. The chipset requires no external components for its operation other than a few...

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#### A two-chip 1.5-GBd serial link interface

Article Full-text available Jan 1993 · IEEE Journal of Solid-State Circuits

Richard C. Walker · C. Stout · J.-T. Wu · [...] · P. Petrino

A silicon bipolar transmitter and receiver chip pair transfers parallel data across a 1.5-GBd serial link. A new 'conditional-invert master transition' code and phase-locked loop that provide adjustment-free clock recovery and frame synchronization are described and analyzed. The packaged parts require no external components and operate over a range of 700 to 1500 MHz using an on-chip VCO. The line code and handshake protoc...

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#### A 1.5 GBaud/sec Serial Link Monolithic Chip Set

Conference Paper Oct 1992 · Microwave Conference, 1992. 22nd European

B. Lai · Richard C. Walker · C. Stout · Jieh Tsong Wu

A 1.5 GBaud/s serial data link comprised of a 2-chip set capable of transporting up to 21 parallel bits was successfully fabricated using a 25 GHz peak ft silicon bipolar process. This link features a new encoding scheme which allows DC balance in the serial stream, as well as an internally generated clock which phase locks to the user's clock at the transmitter, and full clock recovery and data retiming at the receiver. In addition, a...

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#### High Frequency Common Mode Choke

Patent Full-text available Aug 1992

J. Domokos · Richard C. Walker · W. McFarland

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#### Serial extension for 800/1600 Mb/s computer interconnect

Conference Paper Full-text available

Jul 1992 · Communications, 1992. ICC '92, Conference record, SUPERCOMM/ICC '92, Discovering a New World of Communications., IEEE Intern...

C.-S. Yen · Richard C. Walker · W. McFarland · [...] · T. Homak

HIPPI is an ANSI standard (X3.183-1991) for transmitting data in parallel between data processing equipment. To meet the need for transmitting HIPPI data serially on fiber or coaxial cable, serial-HIPPI was created. The authors describe the interface units required by serial-HIPPI, an extender for transmitting data serially between HIPPI nodes at 800 Mb/s or 1600 Mb/s

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#### A bipolar 1.5 Gb/s monolithic phase-locked loop for clock and data extraction

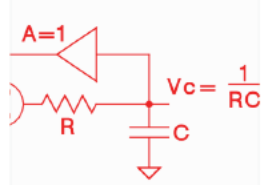
Conference Paper Full-text available Jul 1992 · VLSI Circuits, 1992. Digest of Technical Papers., 1992 Symposium on

J.-T. Wu · Richard C. Walker

The design of a monolithic phase-locked loop (PLL) used in a gigabit serial data link interface for clock and data extraction is described. Implemented in a triple-metal 25-GHz  $f_{t}$  bipolar process and consuming 85 mA from a 5 V-supply, the PLL has a wide frequency acquisition range, from 600 MHz to 1.5 GHz, and a recovered clock phase jitter of less than 18.3 ps r.m.s. The PLL requires only one external...

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### The design and implementation of a chipset for gigabit/second computer networks /

[Article](#) [Full-text available](#) Jul 1992

Richard C. Walker

Thesis (M.S.)—California State University, Chico. Includes abstract. Includes bibliographical references (leaves [48]-51).

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### HP's link interface chipset for Serial-HIPPI

[Conference Paper](#) [Full-text available](#)

Mar 1992 · Comcon Spring '92. Thirty-Seventh IEEE Computer Society International Conference, Digest of Papers.

W. McFarland · Richard C. Walker · C. Stout · [...] · C.-S. Yen

A link interface chipset that conforms to the Serial-HIPPI (High-Performance Parallel Interface) specification is presented. The chipset contains all portions of the link interface and link control functions specified in Serial-HIPPI. The simple additional circuitry required to create a complete Serial-HIPPI link using this chipset is detailed. The two-chip set can also serve as a general-purpose link with no additional circuitry. It transfers...

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### A 2-chip 1.5 Gb/s bus-oriented serial link interface

[Conference Paper](#) [Full-text available](#)

Mar 1992 · Solid-State Circuits Conference, 1992. Digest of Technical Papers. 39th ISSCC, 1992 IEEE International

Richard C. Walker · J.-T. Wu · C. Stout · [...] · P. Petruno

The authors report a monolithic transmitter and receiver chip pair which implements a full-duplex virtual ribbon cable interface. For short-distance applications, on-chip equalizer is provided to allow use of coaxial cables rather than a more costly fiber link. The chips require no external frequency-determining elements or user adjustments and operate over a range of 600 to 1500 MHz using an on-chip VCO (voltage-controlled...

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### A 1.5 Gb/s Link Interface Chipset for Computer Data Transmission

[Article](#) [Full-text available](#) Jul 1991 · IEEE Journal on Selected Areas in Communications

Richard C. Walker · T. Hornak · C.-S. Yen · [...] · Kent H. Springer

The authors designed a set of four ICs to provide encoding, multiplexing, clock extraction/demultiplexing, and decoding for gigabit-rate serial data transmission. These chips form a high bandwidth data link for point-to-point communication. A new line code is implemented that provides DC balance, efficient encoding, framing, and simple clock extraction. Embedded in the code is a fixed transition used by the phase/frequency locke...

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### DC- Free Line Code for Arbitrary Data Transmission

[Patent](#) [Full-text available](#) Jun 1991

Crandall · S. R. Hessel · T. Hornak · [...] · Richard C. Walker

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### Device to block unauthorized modem access over a PBX line

[Patent](#) [Full-text available](#) May 1991

Richard C. Walker · H. Braun

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### Method and Apparatus for Clock Recovery and Data Retiming for Random NRZ data

[Patent](#) [Full-text available](#) Apr 1991

B. Lai · Richard C. Walker

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### A Monolithic 622Mb/s Clock Extraction Data Retiming Circuit

[Conference Paper](#) [Full-text available](#)

Mar 1991 · Solid-State Circuits Conference, 1991. Digest of Technical Papers. 38th ISSCC., 1991 IEEE International

B. Lai · Richard C. Walker

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**Phase Locked Loop for Clock Extraction in Gigabit Rate Data Communication Links**

[Patent](#) [Full-text available](#) May 1990

Corsetto · T. Hornak · R. Nordby · [...] · C.-S. Yen

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**A Fully Integrated High-Speed Voltage Controlled Ring Oscillator**

[Patent](#) [Full-text available](#) Nov 1989

Richard C. Walker

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**A chipset for gigabit rate data communication [using optical fibres]**

[Conference Paper](#) [Full-text available](#) Oct 1989 · Bipolar Circuits and Technology Meeting, 1989., Proceedings of the 1989

Richard C. Walker · T. Hornak · C.-S. Yen · Kent H. Springer

A gigabit-rate data link consisting of four custom silicon bipolar chips for transmitting parallel data between elements of a distributed computer system is discussed. A transmission rate of 16 bits in parallel at 50 MHz or with encoding overhead, a serial rate of 1 Gb/s is demonstrated. The link utilizes an encoding scheme that is bandwidth efficient. Unlike other links, the phase/frequency-locked loop also provides frame...

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**Pseudo-Random Word Sequence Generator and Synchronizer**

[Patent](#) [Full-text available](#) Dec 1988

W. McFarland · Richard C. Walker

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**Gigahertz CMOS/SIMOX circuits**

[Conference Paper](#) Nov 1988 · SOS/SOI Technology Workshop, 1988. Proceedings., 1988 IEEE

J.P. Colinge · J. Kang · W. McFarland · [...] · Richard C. Walker

Summary form only given, as follows. High-speed CMOS logic circuits have been realized in thin-film (100-nm) SIMOX (separation by implantation of oxygen) films annealed at 1250°C. LOCOS (local oxidation of silicon) isolation was used, and the gate oxide thickness was 22 nm. Boron concentration was 1E17 and 5E16 cm<sup>-3</sup> in n- and p-channel devices, respectively. Since no silicide was used, source and drain she...

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**Barclay Tullis**  
Novelthink



**Jeffrey King**  
Corning Incorporated



**C.-S. Yen**  
Not yet on ResearchGate

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**C. Stout**  
Not yet on ResearchGate

Invited



**B. Lai**  
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