

Figure S1

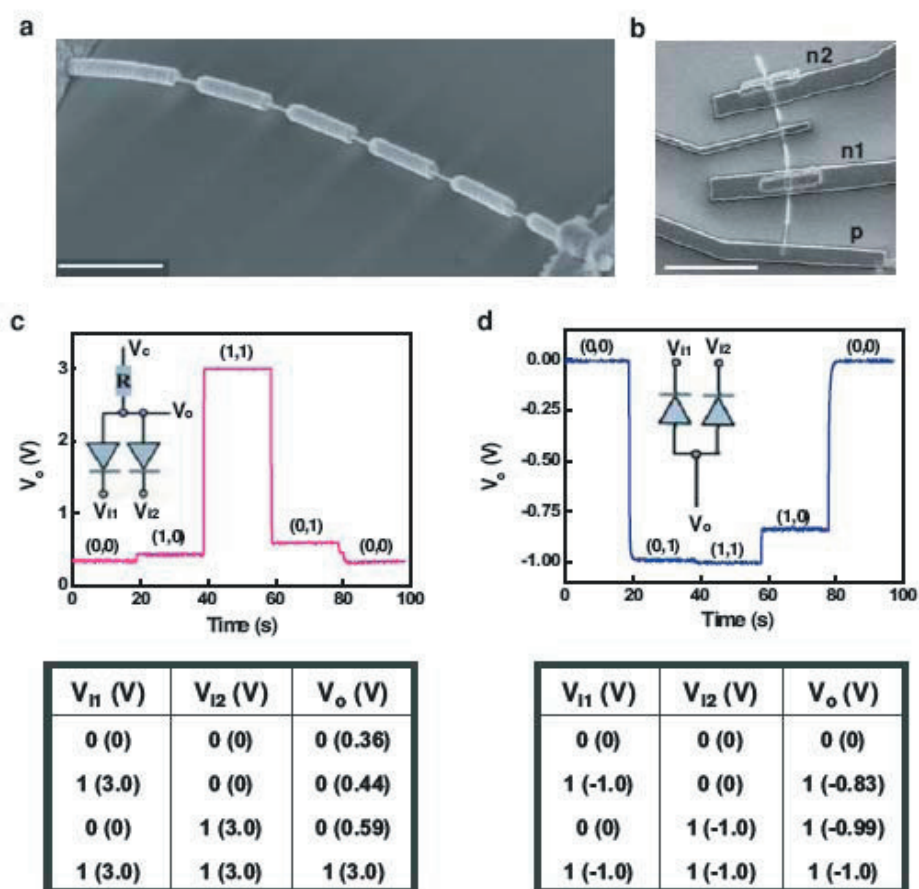


Figure S1 | Periodically etched core/shell SiNW (a) and single NW logic gates (b-d). a, SEM image of the selectively-etched *p-i-n* coaxial SiNW. Scale bar, 2 μm . b, SEM image of the logic gate device, scale bar, 10 μm . Single SiNW AND

(c) and OR (d) logic gates, equivalent circuits (inset of upper panel) and truth tables (lower panel). V_c and R in (c) are 3 V and 25 M Ω , respectively; numbers in parenthesis are measured input and output voltages in the experiments.

Figure S2

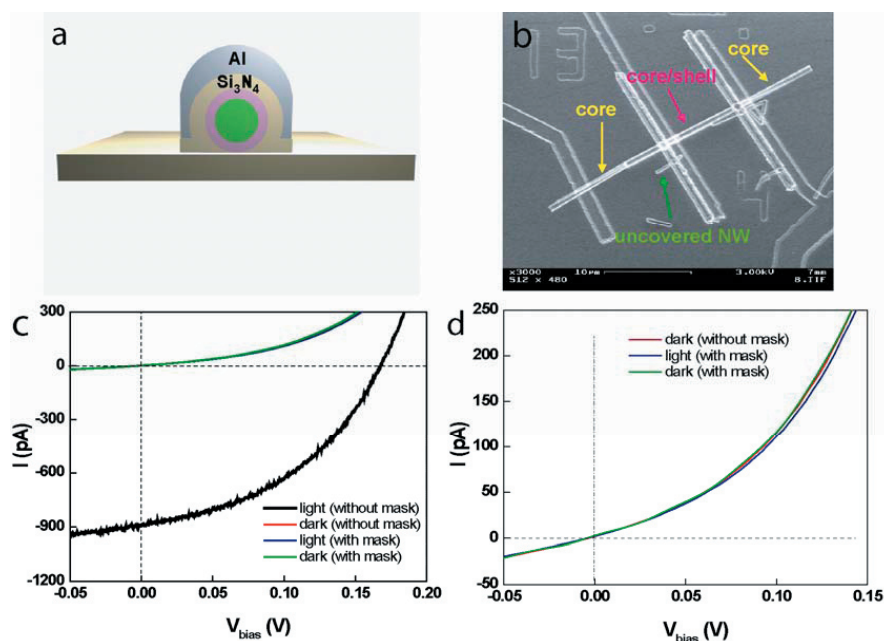


Figure S2 | Nanowire masking experiment. (a) Side-view schematic illustrating the mask structure used in our experiments. Electron beam lithography was used to write a ≤ 800 nm wide slot aligned with the nanowire device, and then 100 nm of Si_3N_4 and 200 nm of Al were deposited over the nanowire. The transmission through the mask is $<1\%$ over the entire region of the solar

spectrum. (b) Scanning electron microscopy image of the masked nanowire device used for the measurements. (c) Illuminated and dark I-V data recorded on the nanowire device with and without Al/ Si_3N_4 mask. (d) Zoom of the illuminated/dark data recorded with the mask and the dark data recorded without the mask.