AN4068

PIC32CM LE00/LS00/LS60 Low-Power Features

Introduction

The Microchip PIC32CM LE00/LS00/LS60 MCUs are ultra low-power Arm® Cortex®-M23 based microcontrollers.

This document describes the low-power optimization features of the PIC32CM LE00/LS00/LS60 family of devices, such as low-power modes (Idle, Standby and Off), Performance Levels, Power Domains, SleepWalking, and Power Gating. This document also includes an MPLAB® Harmony v3-based example illustrating the PIC32CM LE00/LS00/LS60 low-power features.

The application use case is an ADC periodic light conversion triggered by an RTC interrupt, or an RTC event through the Event System. The MPLAB X IDE will be used to load the MPLAB Harmony v3-based example, and the MPLAB Data Visualizer will be used to measure the power consumption and display light sensor activity.

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1. Prerequisites

The following hardware and software are used to illustrate the MPLAB Harmony v3-based example as shown in Low-Power Application Overview.

Hardware Requirements:

- One PIC32CM LE00/LS00/LS60 Curiosity Pro board
- One Microchip I/O1 Xplained Pro Extension Board
- One Micro USB cable

Software Requirements:

- MPLAB X IDE most up to date version
- MPLAB Code Configurator (MCC) for MPLAB Harmony v3 most up to date revision
  - `csp` package
  - `csp_apps_pic32cm_le_ls` package
- MPLAB Data Visualizer (standalone or MPLAB X IDE plugin version)

2. Overview

In many applications, using low power is highly important. In such applications there is a need to balance responsiveness with power consumption. A standard low-power technique is to limit the amount of time a device spends in Active mode by increasing the time spent in low-power sleep modes. The features described in this document enable the device to perform tasks, while in Active mode or in Sleep mode, with very low power consumption.

This document will focus on the available sleep modes, Performance Levels, Power Domains, SleepWalking with or without Power Gating, SRAM, and NVM power management.

This document describes a demonstrative low-power application use case to highlight the key optimization features for low power in the PIC32CM LE00/LS00/LS60 family of devices. The application use case is an ADC periodic light conversion triggered by an RTC event (through the Event System) or an RTC interrupt. The DMA is then used to transfer the sampled data to the internal SRAM. After ten transfers the CPU is woke up by a DMA interrupt to process the data to be plotted into the Data Visualizer through the Data Gateway Interface (DGI) SPI connection.

3. Sleep Modes

Before introducing the features, users need to understand the various sleep modes available in the PIC32CM LE00/LS00/LS60 family of devices. In addition to Active mode, there are three sleep modes in the PIC32CM LE00/LS00/LS60 devices.

For Sleep mode wake-up times, refer to the section “Wake-up Timing” in the Chapter “Electrical Characteristics” in the device data sheet.

3.1 Idle Mode

There is one Idle mode in the PIC32CM LE00/LS00/LS60 family of devices. In this mode, the CPU clock is switched off. The default state of the synchronous AHBx and APBx bus clocks is off, but they can be enabled if requested by the peripherals. For example, if the DMA receives a transfer trigger, it will request its clock signal and start to transfer. By default, the asynchronous Generic Clocks (GCLK_PERIPH) run in Idle mode. Writing the On Demand bit (ONDEMAND) for the corresponding clock source will override this default setting, ensuring GCLK_PERIPH only propagates to a peripheral when requested. Idle mode is entered by executing the Wait For Interrupt (WFI) instruction with IDLE set in the Sleep Mode bit group in the Sleep Configuration register (SLEEPCFG.SLEEPMODE written to 0x2) of the Power Manager (PM) module. The device will exit Idle mode when it detects any non-masked interrupt with sufficient entry priority to cause interrupt entry.

3.2 Standby Mode

In Standby Sleep mode, the device can switch both clocks and power domains on and off. If the device is configured to perform multiple operations in Standby mode, clocks and power domains will only be available when they are needed. This will reduce the overall power consumption.

By default, all clocks except the 32.768 kHz ultra low-power internal RC oscillator (OSCULP32K), are switched off in Standby Sleep mode. Peripherals can still perform tasks if the Run in Standby bit in the peripheral’s CTRLA register (CTRLA.RUNSTDBY) is written to one. This will enable the peripheral to run while in Standby mode. If the clock source is also set to run on demand, the oscillator will only be enabled when requested by a peripheral. Standby mode is entered by executing the WFI instruction with Standby set in the Sleep Mode bit group in the Sleep Configuration register (SLEEPCFG.SLEEPMODE written to 0x4) in the PM module. The device will exit Standby on any asynchronous interrupt.

In Standby mode, by default the device will switch to a low-power voltage regulator (LP VREG) to further reduce the power consumption. Refer to Low Power Voltage Regulator for additional information. For the PIC32CM LE00/LS00/LS60 family of devices, a feature called Power Domain Gating allows dynamic switching of the power domains in Standby mode when available. Refer to SleepWalking with Dynamic Power Domain Gating for additional information.

3.3 Off Mode

In the Off mode the device has no peripherals, voltage regulators, or oscillators running. This mode is entered by executing the WFI instruction with OFF set in the Sleep Mode bit group in the Sleep Configuration register (SLEEPCFG.SLEEPMODE written to 0x6) in the PM module. The only option to wake-up the device is by asserting an external reset on the Reset pin or by a Power-on-Reset (POR).

4. Performance Levels

The PIC32CM LE00/LS00/LS60 family of devices can operate at two performance levels. When operating from the lowest level PL0, the voltage applied on the full logic is reduced by voltage scaling. This voltage scaling technique allows to reduce the active power consumption while decreasing the maximum frequency of the device. On the highest performance level PL2, the voltage regulator supplies the highest voltage, allowing the device to run at higher clock speeds.

4.1 Changing Performance Level

Switching to a different performance level does not affect oscillators, prescalers, or GCLK generators. After changing to a higher performance level, it is necessary to wait for the Performance Level Ready bit in the Interrupt Flag Status and Clear register (INTFLAG.PLRDY) in the PM module to be set before changing the clock speed.

Before reducing the performance level, the bus frequency must be reduced to avoid exceeding the limit of the target performance level. It may also be necessary to change the number of read wait states which is dependent of the CPU clock speed, performance level, and VDDIN voltage. For additional information, refer to the Chapter “Electrical Characteristics” in the specific device data sheet.

The number of read wait states is configured by writing to the NVM Read Wait States bit group in the Control B register (CTRLB.RWS) in the Non-Volatile Memory Controller (NVMCTRL). Increasing the number of wait states must be done before changing the performance level. Similarly, decreasing the number of wait states must be done after changing the performance level. The following examples demonstrate how to change the performance level:

Changing to a lower performance level (PL0 mode) when running at higher than 12 MHz (PL2 mode):

1. Disable or decrease clock generators above the maximum allowed frequency (12 MHz).
2. Choose PL0 as performance level (PLCFG.PLSEL written to 0x0) in the Power Manager.
3. The number of wait states must be decreased depending on the new CPU speed:
   For additional information, refer to the Section “NVM Characteristics” in the Chapter “Electrical Characteristics” of the specific device data sheet.

Changing to a higher performance level (PL2 mode) when running at 12 MHz or lower (PL0 mode):

1. The number of read wait states must be increased depending on the new CPU speed:
   For additional information, refer to the Section “NVM Characteristics” in the Chapter “Electrical Characteristics” of the specific device data sheet.
2. Choose PL2 as performance level (PLCFG.PLSEL written to 0x2) in the PM.
3. Wait for the Performance Level Ready Flag bit (INTFLAG.PLRDY) to be set in the PM. An interrupt is generated when the PLRDY Flag bit occurs while the Performance Level Ready interrupt is enabled in the PM Interrupt Set register (INTENSET.PLRDY written to one).
4. Increase the CPU clock speed without exceeding the maximum allowed frequency.

4.2 Voltage Regulator System

The PIC32CM LE00/LS00/LS60 family of devices can operate from one of the several internal voltage regulators. The main voltage regulator (Main VREG) supplies the core domain (VDDCORE) when the device is in Active mode or Idle Sleep mode. In Standby Sleep mode, VDDCORE is either powered by Main VREG or the low-power voltage regulator (LPVREG). The PIC32CM LE00/LS00/LS60 series of devices also embeds a PLL/DFLL domain (VDDPLL), which is powered by the PLL Voltage Regulator (VREGPLL).

4.2.1 Main Voltage Regulator

The main VREG can be supplied by two voltage regulators: an LDO and a Buck switching regulator. The Buck switching regulator will consume the least amount of power, having the highest efficiency of the two in Active mode. However, the buck switching regulator requires an inductor to be connected to the device. Since this inductor is not guaranteed to be available in all designs, the PIC32CM LE00/LS00/LS60 family of devices will by default start from the LDO regulator. Switching between the LDO regulator and the Buck switching regulator is done by writing

to the Voltage Regulator Selection bit in the Voltage Regulator System Control register (VREG.SEL) in the Supply Controller (SUPC).

4.2.2 PLL Voltage Regulator

The PLL Voltage Regulator (VREGPLL) is used to power the VDDPLL domain. If one of the FDPLL96M, DFLL48M or DFLLULP clock sources must be used by the application, the user must enable the VREGPLL regulator. These clock sources must be enabled only when the VDDPLL supply is established. When enabled, the VREGPLL regulator remains enabled in all sleep modes, except Standby mode (where the regulator supports the Sleep Walking capability), and Off mode.

4.2.3 Low-Power Voltage Regulator

The Low-Power voltage regulator can be used to supply VDDCORE during Standby mode, if the VREG Switching mode is set to Low-Power mode (STDBYCFG.VREGSMOD written to 0x2), or if the VREG Switching mode (STDBYCFG.VREGSMOD written to 0x0) is set in the Power Manager.

The efficiency of LPVREG can be improved by setting the Low-Power mode Efficiency bit in the VREG register (VREG.LPEFF written to 0x1) in the Supply Controller for applications where a limited VDD range (2.5V to 3.63V) is used.

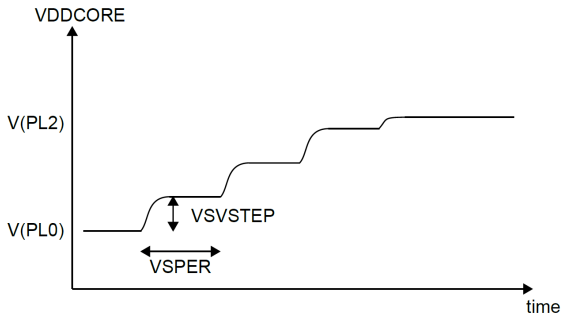
For additional information, refer to the Section “Power Domains”of the Chapter “Power Manager”in the specific device data sheet.

4.2.4 Voltage Scaling Control

The VDDCORE supply will change under certain circumstances, such as switching to a different performance level, entering, or exiting Standby, or when a SleepWalking task is started. A sudden VDDCORE increase can cause a spike in the current flow. Forcing the regulator to make a softer transition of voltage levels by writing to the Voltage Scaling Step and Voltage Scaling Frequency bit group in the Voltage Regulator System Control register (VREG.VSSTEP and VREG.VSPER in the SUPC module) will limit such current spikes. However, it will also increase the total step time. For additional information, refer to the following figure. The transition time can be decreased by configuring a larger voltage step height since the number of steps are reduced. By default, VSVSTEP is written to 0x0 giving a step height of 5mV. The scaling frequency VSPER determines the delay between the steps. By default, VSPER is written to 0x0 giving a delay of 1 µs.

In designs where the power supply is weak, and if powered by a nearly discharged battery, a softer transition may prevent the external power supply voltage level from dropping below the BOD threshold value. The current spikes only affect the external power supply and not the device as long as the external power supply manages to source the necessary current flow.

Figure 4-1. Voltage Scaling



Note: When VREGPLL is enabled, the VSVSTEP and VSPER settings also apply to VREGPLL.

5. Power Domains

Power Domains allow power saving by limiting or powering off logic areas in the device. Most of the power domains can switch between the following three states:

- **Active state:** Peripherals in the power domain are powered and ready to be used or configured
- **Retention state:** Main voltage supply is powered off while maintaining a low-power supply to hold the state of the registers and SRAM
- **Off state:** Peripherals in the domain are not powered and registers must be reprogrammed for a peripheral to be used

Turning power domains off or using a retention state allows the device to consume less power in Standby than what is achievable by only disabling clocks. Power domains are automatically switched between active and retention state, but can also be forced to active state. The dynamic switching is known as Power Domain Gating. Power domain configurations are set in the Standby Configuration (STDBYCFG) register in the Power Manager module.

The PIC32CM LE00/LS00/LS60 family of devices have three power domains (PDAO, PDSW, and PDPLL) other than the supply domains, such as VDD, and AVDD. For Power Domain Partitioning details, refer to the Chapter “Power Manager” in the specific device data sheet.

5.1 PDAO

The PDAO contains all controllers located in the Always-On domain, for example, the PM, Reset Controller, Supply Controller, Real-Time Counter, External Interrupt Controller, Analog Comparator, PORT controller, and the 32 kHz Oscillator Controller. It is powered when in Active mode, Idle mode, or Standby mode.

5.2 PDSW

The PDSW is a switchable power domain which contains the Event System, Generic Clock Controller, Main Clock Controller, Oscillator Controller, NVMCTRL, DMA Controller, Device Service Unit, and Arm Cortex-M23 core. The PDSW also contains the following peripherals that enable the device to wake up from an interrupt: SERCOM, Timers, ADC, DAC, OPAMP, CCL, PTC, TRNG, USB, and I^2S. In Standby mode, PDSW can be turned off to save leakage consumption according to the user configuration.

5.3 PDPLL

The PDPLL is the PLL power domain. It contains the FDPLL96M, DFLL48M, and DFLLULP clock sources. In Standby mode, it can be turned off to save leakage consumption according to the user configuration. Depending on the peripheral settings, the FDPLL96M and DFLL48M can be switched off if no clock activity is required.

6. Advanced Features

6.1 SleepWalking

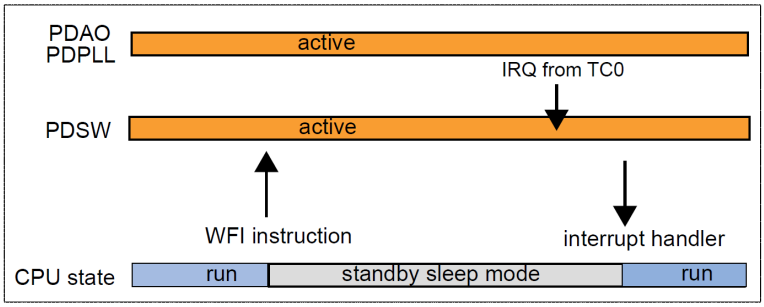
SleepWalking is the capability for a device to temporarily wake up clocks for a peripheral to perform a task without waking up the CPU from Standby mode. At the end of the SleepWalking task, the device can either be woke up by an interrupt (from a peripheral involved in SleepWalking) or reenter into Standby mode. The SleepWalking is supported only on the GCLK clock by using the on-demand clock principle of the clock sources.

6.1.1 SleepWalking with Static Power Domain Gating

In Standby mode, the switchable power domain (PDSW) of a peripheral can remain in active state to perform the peripheral's tasks. This Static Power Domain Gating feature is supported by all peripherals. For some peripherals, it must be enabled by writing the Run in Standby bit in the respective Control A register (CTRLA.RUNSTDBY written to 0x1).

The following figure illustrates the state of the Power Domains and CPU with Static Power Domain Gating:

Figure 6-1. SleepWalking with Static Power Domain Gating Example

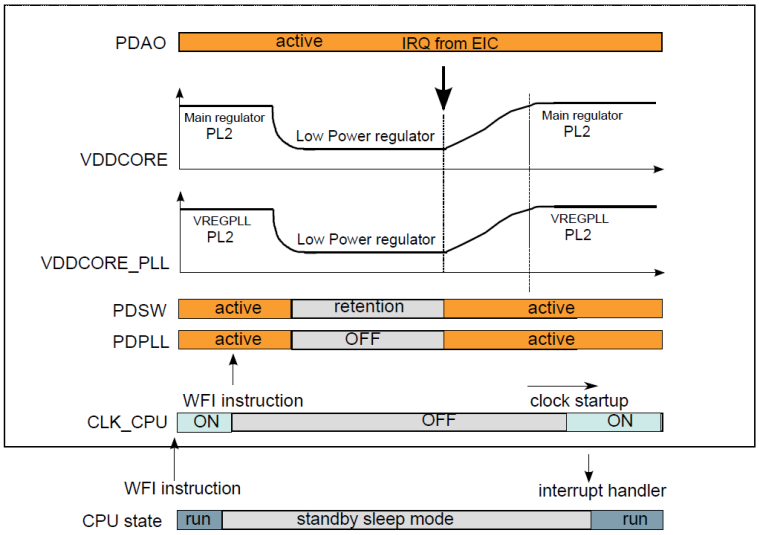


6.1.2 SleepWalking with Dynamic Power Domain Gating

The SleepWalking feature extends the capability of setting the switchable power domain from retention to active and vice-versa. This means a power domain will only be active when a peripheral needs to run. This is called Dynamic Sleepwalking. To apply this feature based on events or DMA triggers, the Dynamic Power Gating bit in the Standby Configuration register (STDBYCFG.DPGPDSW) in the PM must be set to 0x1. When a SleepWalking task activates a power domain, this is done without waking up the CPU. When the task is complete, the device can either wake up if an interrupt is issued or return to Standby mode.

The following figure illustrates the state of Power Domains and CPU with Dynamic Power Domain Gating:

Figure 6-2. SleepWalking with Dynamic Power Gating Example



6.2 SRAM Back-Biasing Mode

By default, the SRAM is in Low-Power mode (back-biased), if its power domain is in a retention state and the device is in Standby mode.

This behavior can be changed by configuring the BBIASxx bit groups in the Standby Configuration register (STDBYCFG.BBIASxx):

Table 6-1. SRAM Back-Biasing Mode

Value	STDBYCFG.BBIASxx Configuration	SRAM
0x0	Retention Back Biasing mode	SRAM is back-biased if its power domain is in retention state.
0x1	Standby Back Biasing mode	SRAM is back-biased if the device is in Standby Sleep mode.

6.3 SRAM Power Switch

The SRAM is divided into sub-blocks, which can be switched off to optimize power consumption. By default, all sub-blocks are retained, but it is possible to switch them off depending on the SRAM memory size. This behavior can be changed by configuring the RAMPSWC bit groups in the Power Configuration register (PWCFG.RAMPSWC) in the PM module.

6.4 NVMCTRL Power Management

The NVMCTRL will continue to operate in any sleep modes where the selected source clock is running. The NVMCTRL interrupts can be used to wake up the device from sleep modes.

The Power Manager will automatically put the NVM block into a low-power state when entering Sleep mode. This is based on the SLEEPPRM bit in the Control B register (CTRLB.SLEEPPRM) in the NVMCTRL module.

The NVM Read mode can be in low power to reduce the power consumption of the cache memory. This can be set by writing the READMODE bit field in the Control B register (CTRLB.READMODE) to 0x1 in the NVMCTRL module.

For additional information, refer to the Chapter “NVMCTRL” in the specific device data sheet.

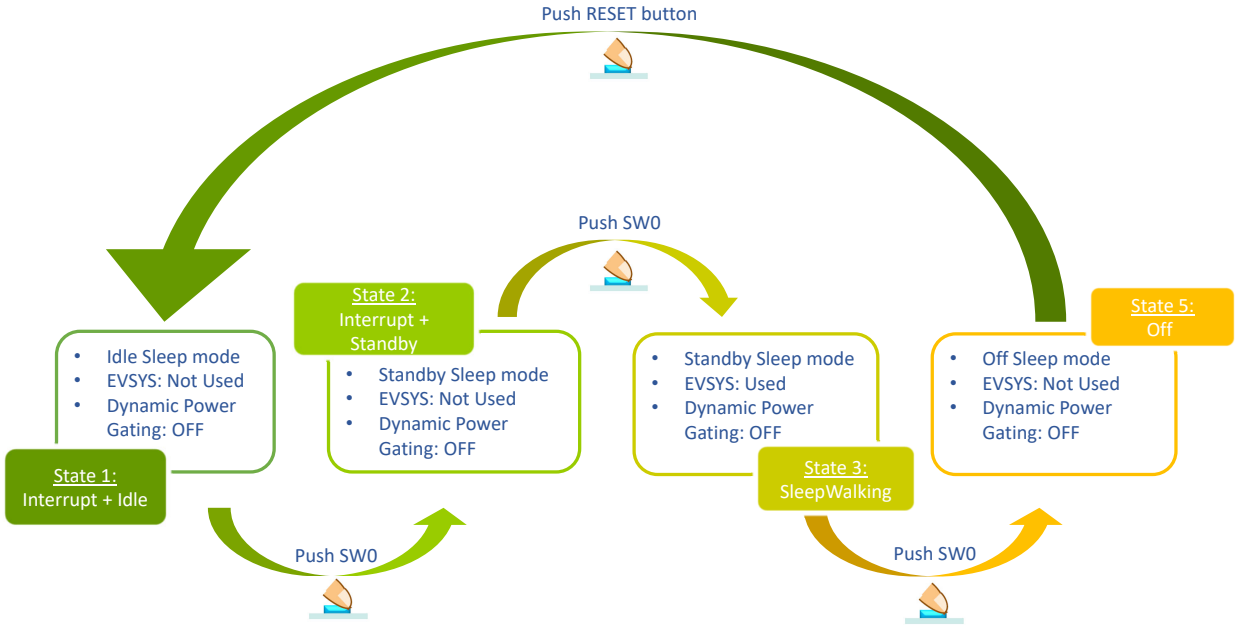
7. Low-Power Application Overview

7.1 State Machine Block Diagram

To have a clear picture of the differences in terms of power consumptions, a demonstration is implemented using a state machine in the application. Using the SW0 button, the user can browse the different implementations previously described, and easily measure the resulting power consumption.

The following figure illustrates a description of the implemented state machine:

Figure 7-1. PIC32CM LE00/LS00/LS60 Low Power Features Example - State Machine Block Diagram



The goal is to compare different application implementations in terms of power consumption. The following implementations proposed:

- Interrupt in Idle mode
- Interrupt in Standby mode
- SleepWalking with Static Power Gating
- Off mode

In each of those implementations (except Off mode) the main application remains the same and is introduced as follows:

- RTC is configured as a trigger source to start the ADC
- ADC starts a conversion of the light sensor of the Microchip I/O1 Xplained Pro Board
- DMA moves the conversion from the ADC RESULT register to the internal SRAM
- After 10 transfers, the DMA generates an interrupt to wake-up the core and process the data
- Data is then sent to the Data Visualizer using the embedded debugger Data Gateway Interface (DGI) SPI
- Power consumption can be directly measured through the MPLAB Data Visualizer

Note: The Data Gateway Interface (DGI) allows the low-level transport of data to and from a target MCU through a USB interface. DGI provides several interfaces that implement an abstraction to a physical communication interface, such as UART, I^2C, or SPI.
In this application the DGI SPI is used to transport light level values coming from I/O1 Xplained Pro light sensor. These values are then displayed on Data Visualizer as a graph.

7.1.1 Opening the Low-Power Features Example from MPLAB Harmony v3

The code example is available in the MPLAB Harmony v3 Framework repository.

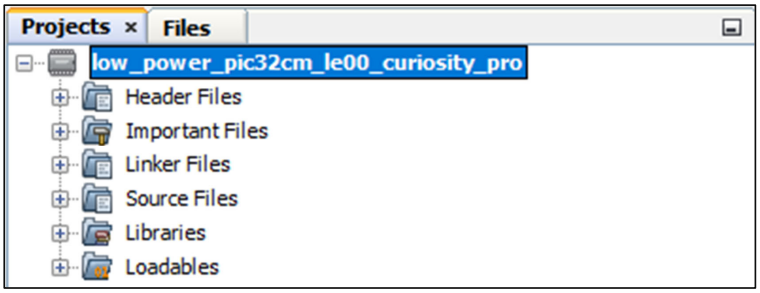
Note: Ensure that the MPLAB Harmony v3 Framework is installed, and the user can download the folder using the MPLAB Code Configurator (MCC) Content Manager. If MPLAB Harmony framework is not installed while opening an MCC project, the required packages will be downloaded (default folder path is *C:/Users/HarmonyFramework*).

Follow these steps to open the software project:

1. Open MPLAB X IDE.
2. Select *Toolbar > File > Open Project (Ctrl + Shift + O)*.
3. Open the appropriate `low_power_features` example:
   a. Navigate to *C:\<Harmony3_Framework_Path>\csp_apps_pic32cm_le_ls\apps\pm for PIC32CM LE00*.
   b. Navigate to *C:\<Harmony3_Framework_Path>\csp_apps_pic32cm_le_ls\apps\trustZone\pm for PIC32CM LS00/LS60*.

   Once opened, the `low_power_features` example must appear in the MPLAB X IDE Project Tree:

Figure 7-2. Low Power Features Project Tree Under MPLAB X IDE for PIC32CM LE00



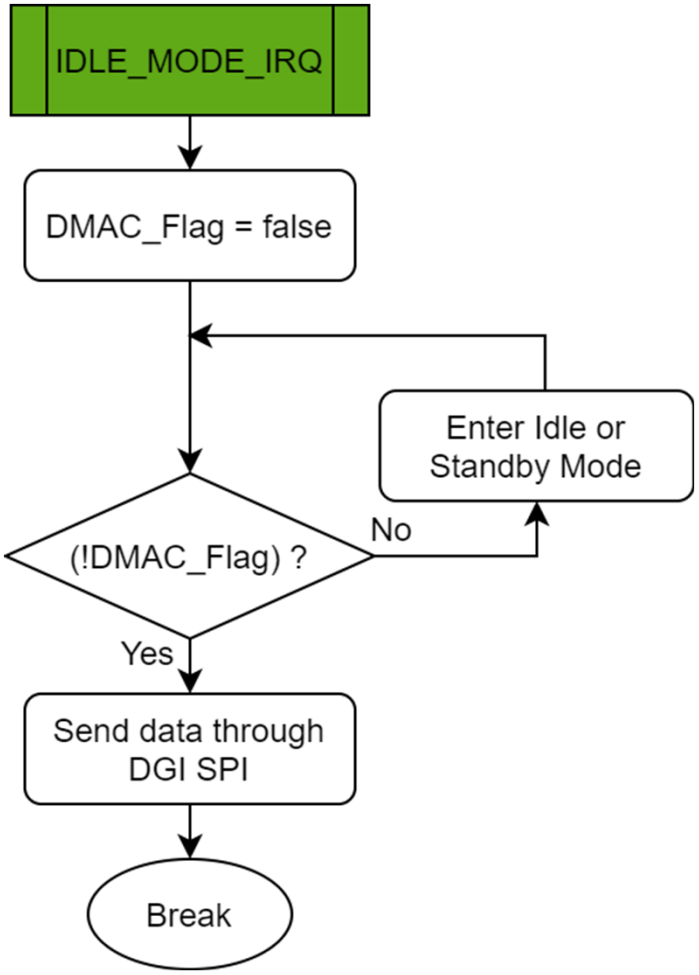
7.2 Application Modes Flowcharts

7.2.1 Application STATE 1 & 2: Interrupt-Based Application Flowchart

The interrupt-based application is applied for STATE 1 (Interrupt + Idle) and STATE 2 (Interrupt + Standby). Whether in STATE 1 or STATE 2, the CPU is woken up every 100 ms using an RTC interrupt (based on the OSCULP32K) to start the ADC conversion.

At the end of a 10-transfer frame, the CPU is woken up using a DMA interrupt to process the data to be plotted into the Data Visualizer through the DGI SPI connection.

Figure 7-3. Application STATE 1 or 2: Interrupt-Based Application Flowchart

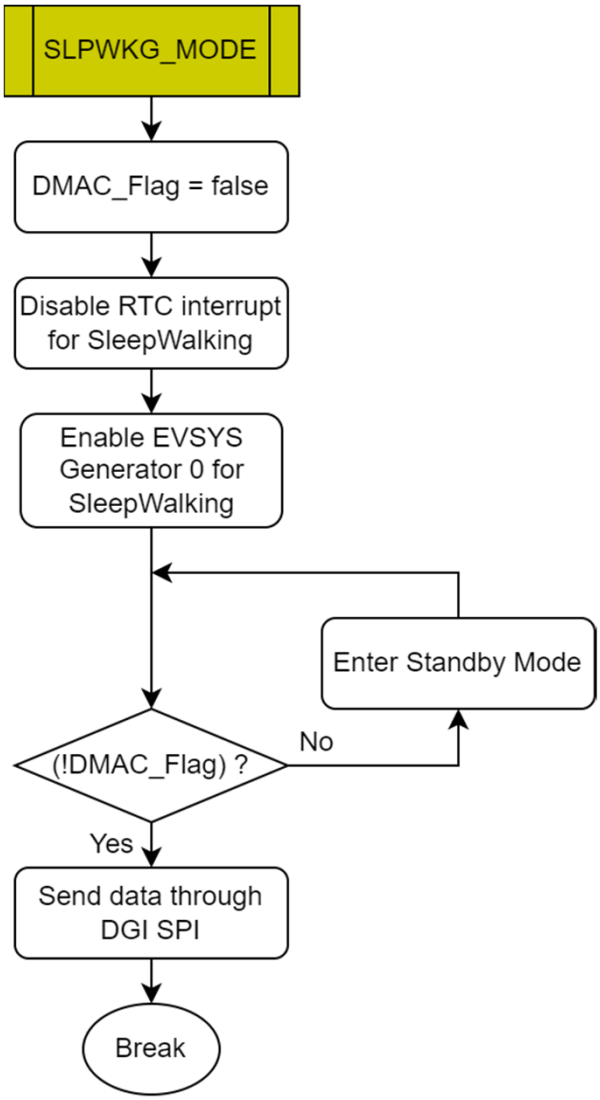


7.2.2 Application STATE 3: SleepWalking-Based Application Flowchart

In STATE 3, Standby mode is used upon events controlled by the EVSYS module to benefit from the PIC32CM LE00/LS00/LS60 architecture. The last interrupt, triggered by the DMA, is used to wake up the CPU to process the data to be plotted.

The RTC will automatically start the ADC conversion using the Event System of the chip, without any CPU intervention. The ADC will then convert the analog signal coming from the light sensor, and it will trigger a DMA data transfer to the internal SRAM immediately the result of the conversion is ready. This part is automatically done by an internal hardware trigger path between the ADC and the DMA.

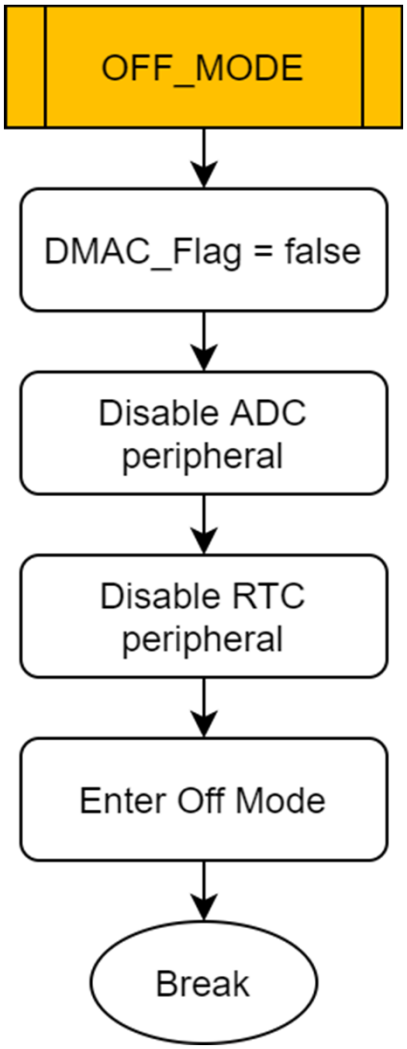
Figure 7-4. Application STATE 3: SleepWalking Based Application Flowchart



7.2.3 Application STATE 4: Off Application Flowchart

In this implementation, the device is completely powered Off. To recover from this Sleep mode, push the on-board mechanical RESET button.

Figure 7-5. Application STATE 4: Off Mode Application Flowchart



7.3 Low-Power Application Outputs and Results

The application use case is configured to send data through the DGI SPI connections of the device every second. Then users can connect the DGI SPI device outputs to the MPLAB Data Visualizer tool to display the environmental light measured by the I/O1 Xplained Pro. The Data Visualizer can be used to display the power consumption of the device for each low-power mode.

7.3.1 DGI SPI Output

The following figure shows an example of data that can be displayed by the Data Visualizer when the application is running on Interrupt or SleepWalking-based applications. Because the entire device is turned OFF while running in Off mode, the DMA stops sending data through the DGI SPI and there is no new value that is displayed on the Data Visualizer until the device is RESET mechanically.

Figure 7-6. DGI SPI Output

Note: The DGI SPI Endpoint must be configured with the `DataStream_Configuration_File.txt` file provided along with the code example to display the measured light.

Note: Any Lamp or Torch app utility can be used, and is available on most smart devices to play the demonstration. The light sensor activity is available in all the application states (except STATE 4).

7.3.2 Power Consumptions

When the application is running, the current consumption of the application can be measured with the MPLAB Data Visualizer tool using the Power Analysis feature.

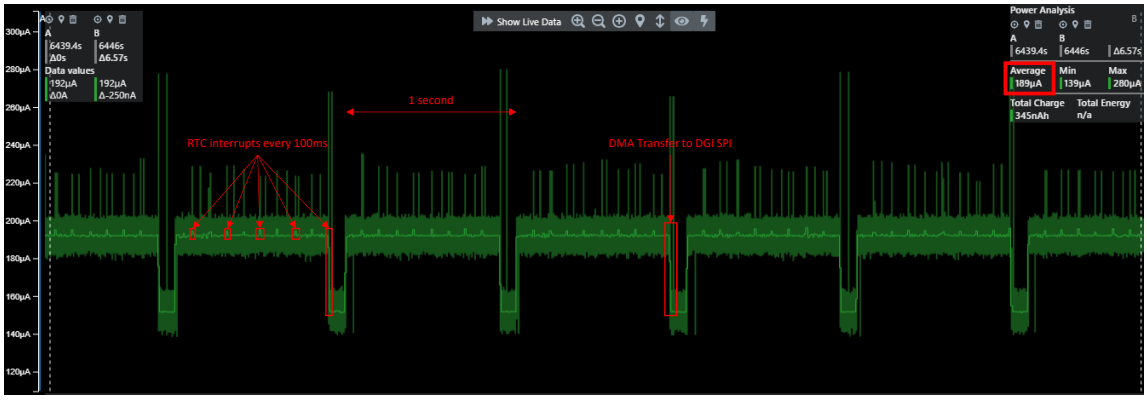
Notes:

1. The average value must be considered while measuring the power consumption of the application.
2. The values, provided in Figure 7-7 to Figure 7-10, were measured on the PIC32CM LE00 Curiosity Pro board.
3. The power is measured with the following Power Manager peripheral's configuration:
   - PL2 mode (PM (PLCFG.PLSEL = 0x2))
   - PDSW power domain is forced active (PM (STDBYCFG.PDCFG = 1))
   - Low-Power mode efficiency is enabled (SUPC (VREG.LPEFF = 0x1))

Application State 1: Interrupt in Idle mode

The following figure shows the power consumption of the device when running on Interrupts in Idle mode:

Figure 7-7. Interrupt + Idle Mode Power Consumption

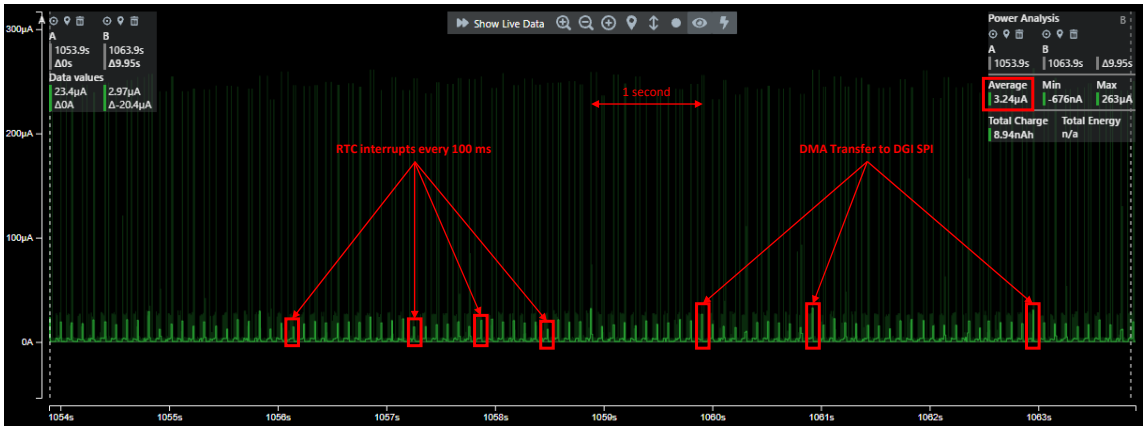


Note: The average power consumption measured in Interrupt + Idle mode is 189 µA.

Application State 2: Interrupt in Standby mode

The following figure shows the power consumption of the device when running on Interrupts in Standby mode:

Figure 7-8. Interrupt + Standby Mode Power Consumption



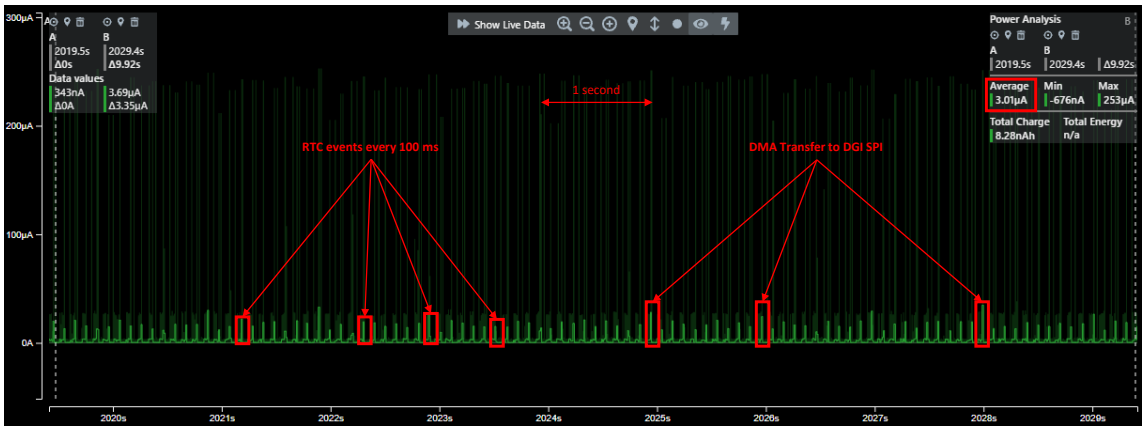
Notes:

1. The average power consumption measured in Interrupt + Standby mode is 3.24 µA.
2. The power consumption measured is obtained with the external 12 MHz oscillator disconnected, to remove its own power consumption. Refer to the *PIC32CM LE00/LS00/LS60 Curiosity Pro Board Change Notification (DS70005491)* for additional information.

Application State 3: SleepWalking with Static Power Gating

The following figure shows the power consumption of the device when running on SleepWalking with Static Power Gating:

Figure 7-9. Sleepwalking with Static Power Gating Power Consumption



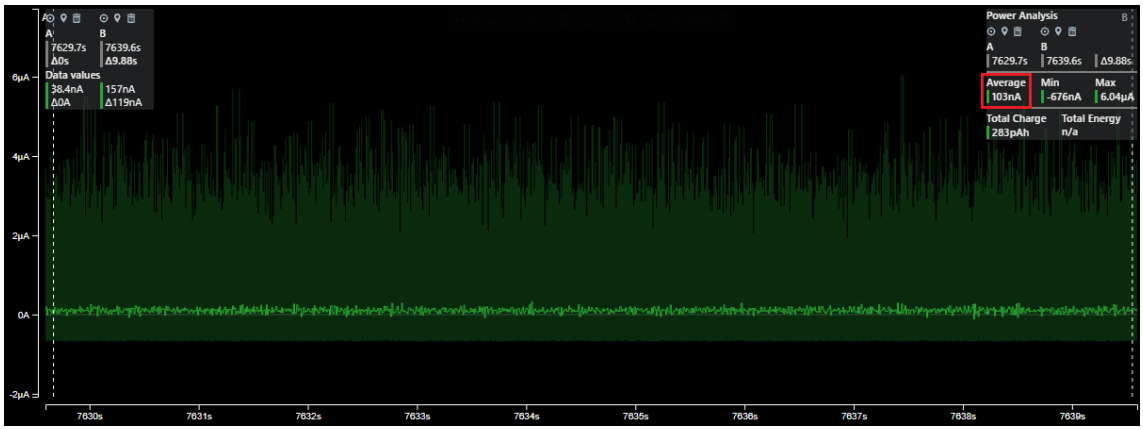
Notes:

1. The average power consumption measured in Sleepwalking (Standby + Events) with Static Power Gating mode is 3.01 µA.
2. The power consumption measured is obtained with the external 12 MHz oscillator disconnected, to remove its own power consumption. Refer to the *PIC32CM LE00/LS00/LS60 Curiosity Pro Board Change Notification (DS70005491)* for additional information.

Application State 4: Off Mode

The following figure shows the power consumption of the device when running in Off mode:

Figure 7-10. Off Mode Power Consumption



Notes:

1. The average power consumption measured in Off mode is 103 nA.
2. The power consumption measured is obtained with the external 12 MHz oscillator disconnected to remove its own power consumption. Refer to the *PIC32CM LE00/LS00/LS60 Curiosity Pro Board Change Notification (DS70005491)* for additional information.

8. Conclusion

The PIC32CM LE00/LS00/LS60 family of devices offers several low-power features. The following points were highlighted throughout the document:

- Familiarity with the PIC32CM LE00/LS00/LS60 Curiosity Pro Board.
- Benefits of the PIC32CM LE00/LS00/LS60 Sleep Modes.
- Performance Levels and Power Domains.
- Advanced low-power features, such as SleepWalking, SRAM Back-Biasing, Power Switch, and NVMCTRL Power Management.
- Familiarity with the Microchip development tools, such as MPLAB X IDE, MPLAB Code Configurator for Harmony v3, and MPLAB Data Visualizer.

9. References

For additional information, refer to the following documents which are available for download at Microchip website:

- PIC32CM LE00/LS00/LS60 Family Data Sheet (DS60001615)
- PIC32CM LE00/LS00/LS60 Family Silicon Errata and Data Sheet Clarifications (DS80000906)
- PIC32CM LE00/LS00/LS60 Curiosity Pro User Guide (DS70005443)
- PIC32CM LE00/LS00/LS60 Curiosity Pro Board Change Notification (DS70005491)

10. Revision History

Revision C - 03/2022
The following updates were performed on this document:

- Removed an erroneous bulleted item for Sleepwalking with Dynamic Power Gating in the State Machine Block Diagram
- Added a new note to Power Consumptions
- Replaced Figure 7-8, and 7-9 in Power Consumptions
- Added a new section titled Application State 4: Off Mode to Power Consumptions
- Added a new references to the References section

Revision B - 01/2022
The following updates were performed on this document:

- Updated VDDCORE_PLL to VDDPLL throughout the document
- Updated VDDIO to VDD throughout the document
- Updated steps 1-3 of Opening the Low-Power Features Example from MPLAB Harmony v3
- Updated Application STATE 3: SleepWalking-Based Application Flowchart with a new figure

Revision A - 04/2021
This is the initial release of this document.

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