ABSTRACT

The technological developments made over the last few decades have created the possibility to fabricate electronic devices on a nano-meter scale. The physics of these small devices is dominated by quantum mechanics. In this project, two dimensional electron gas and one dimensional electron gas samples were fabricated and measured. The project work involved a thorough analysis and explanation of the electron transport in such mesoscopic systems, covering the fundamental characteristic effects observed in these systems, such as the quantum Hall effect in the 2D systems and the quantized conductance effect in quasi-1D devices.

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INTRODUCTION

Nanotechnology has been a challenging research area because of the fabrication and processing carried out for developing meso-scopic systems; however this is extremely rewarding because of the dimensionality playing an important role in determining the properties of materials, for example the ways of electron interactions in three-dimensional, two-dimensional (2D) and one-dimensional (1D) structures [1-3]. Due to major advances being made in lithographic technology, it has enable researchers to fabricate nano-scale structures which have great control over electron transportation. For performing quantum observations of low-dimensional electron transport, firstly one has to make sure the thermal energy must be less than the electron energy-level spacing which is achieved by combination of temperatures less than 1 K (-272 ^{o}C) and device dimensions less than one micron. Secondly, motion of electron must be ballistic, meaning no scattering of electrons within the transport medium [4]. Among different quantum devices, simplest is a two-dimensional electron gas where the electron gas (2DEG) is confined in one direction and is free in the other two. This confinement is achieved by forming *heterojunctions* between two different band gap semiconductor lattices. Most common and widely explored of all is GaAs/AlGaAs (1.42 eV and 2eV respectively) heterojunction structures because of the potential of high mobilities that can be achieved by varying growth parameters [5-8]. The band diagram of a two-dimensional heterostructure is as shown in figure (a), from the band diagram one can see that due to low-confinement, the electrons occupy discreet energy bands called 'sub-bands' and this results into quantized motion of electrons in a quasi-2D channel as shown by Shubnikov-de Haas Oscillations [9-10].
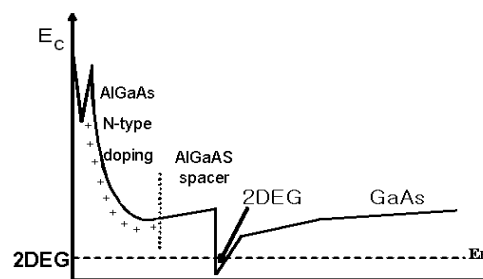
Figure (a) Band diagram of 2DEG formed

Confinement in further dimensions leads to development of nano-structures such as quantum wires and dots. This is usually achieved by patterning point contacts called Sharvin contacts [11] fabricated by electron beam lithography (EBL). When the negative bias is applied to this gates it depletes electrons from the 2DEG lying underneath the electrodes. This ballistic transport in quasi-one dimensional channel results in quantum corrections of quantized conductivity as observed in 2DEG [20].

CHAPTER ONE: FABRICATION OF 2DEG HEMT STRUCTURES

1.1 Introduction

The chapter talks about the fabrication technique that was implemented and enhanced later on in processing HEMTs devices which was based on conventional HEMT processing technique for GaAs substrates. The process starts from Epitaxial growth of the heterostructures on the substrates, then in order to form a layer of 2DEG near the GaAs substrate-AlGaAs spacer layer the epitaxially grown devices need to be processed further which results into isolation of two terminal semiconductor mesa from the substrate and is sequentially carried out by Lithography and Etching process. And finally metal contact pads are deposited using conventional Metallization technique.

1.2 Epitaxial growth of Heterojunction super-lattices

The confinement of 2DEG highly depends on this process as the collection of the electrons near the AlGaAs spacer layer and substrate relies on the thickness of spacer layer formed and the amount of n-doping in the AlGaAs. The heterostructures are carefully grown layer by layer using MBE (Molecular Beam Epitaxy) which allows producing atomically smooth layers with precise control over layer thickness, an example is shown in figure 1.1. It also controls the doping level of impurities added to semiconductor layer and tuning these parameters while growth can improve the performance of the device. As for Si doped GaAs-AlGaAs semiconductor devices mobilities similar to that undoped GaAs device is difficult to achieve because of the additional donor impurities in former device hindering the motion of confined electron gas.
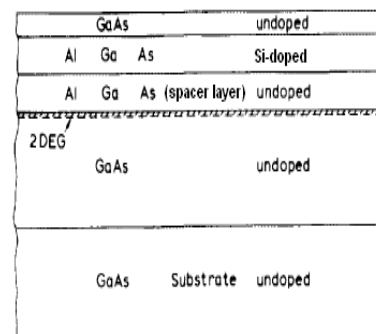
However previous work has shown that by modulated doping concentration of Si in AlGaAs layer the donor impurities can be isolated from the confined electron gas resulting into considerably high mobility for the electron gas and electron concentration equivalent to bulk GaAs is obtained [12-13], figure 1.2 shows Energy band diagrams of undoped and n-doped GaAs/AlGaAs superlattices. For the samples fabricated during the course of the project the doping concentration of Si in AlGaAs was maintained around 2E18 cm^{-3}, and the AlGaAs spacer layer thickness was altered (20 nm, 40 nm, 60 nm) in order to maximize the mobility as this is the parameter which separates ionized impurities from 2DEG and hence can improve performance of the device.
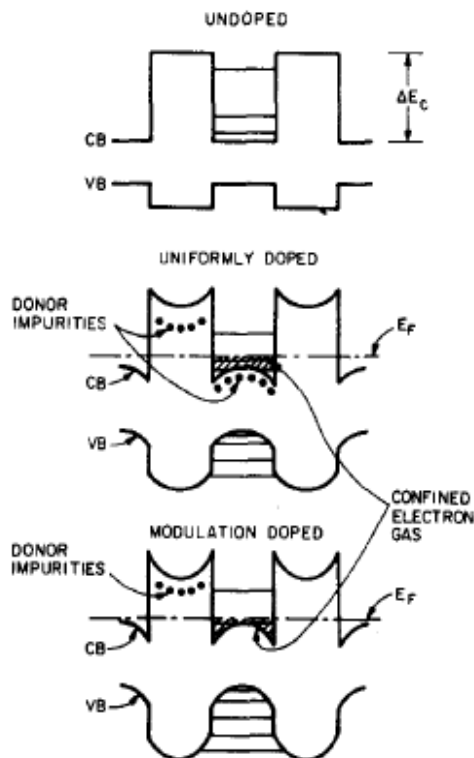
Figure 1.2 Energy band diagrams for doped and undoped GaAs/AlGaAs superlattices

1.3 Formation of semiconductor mesa, isolated from substrate

As mentioned before formation of semiconductor channel included following activities:

- Conventional Optical Lithography
- Wet Etching

1.3.1 Conventional Optical Lithography

In order to form Hall Bar channel for conduction of electrons on the semiconductor mesa, pattern of Hall Bar onto the substrate needs to be developed. This is done by implementing time-efficient optical lithography process which in this case is used for pattering large areas such as Hall Bars in first round and then Metal contacts at the terminal of Hall Bars in second round.

For patterning Hall Bar mesas negative photo resist (Shipley 1813) was spun over the wafer sample at 5000 rpm for 30 sec which gave thickness of resist deposited of 1.2 μm similar to what can be achieved in resist datasheet as shown in **appendix A**. This was then followed by soft bake of resist in order to improve its adhesion at 115 ^{o}C for 60 sec. The pattern was then exposed to Ultraviolet radiation for 7 sec. The photo resist pattern was then developed by Microposit MF-319 developer for 60 sec followed by rinsing with IPA (isopropyl alcohol) and water, and is as shown in figure 1.3
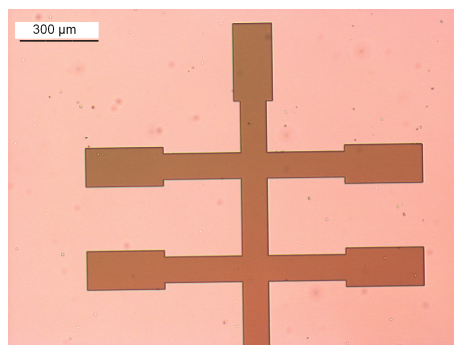

Figure 1.3 Hall bar patterned on photo-resist due to optical exposure

The height of the resist pattern was then measured using Alpha-Step IQ, stylus-based surface profiler. And the surface profile measured is as shown in figure 1.4
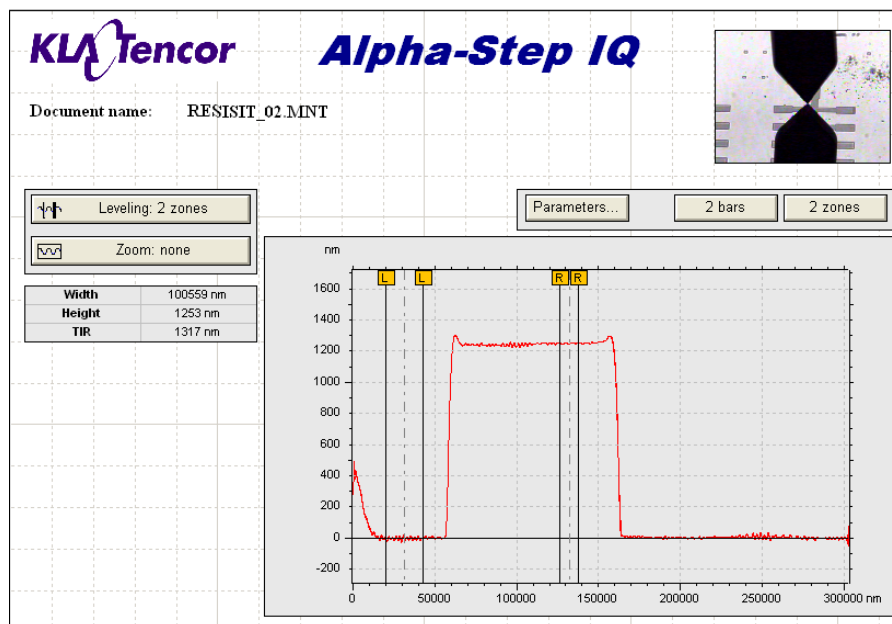

Figure 1.4 Measurement of surface profile using Alpha-Step IQ

1.3.2 Wet Etching

After looking at the surface profile of the resist pattern, wet etching is followed and the etchant used during the course of project for different sample wafers was a mixture of DI (deionised) water, sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). The ratio of these components and time for which samples was immersed in etching solution were crucial factors in determining the height of the sample mesa to be etched. For e.g. for one of the sample with 20 nm spacer layer, the amount of etching height needed to make direct contact with unetched 2DEG with metallic contacts is 70nm. The required etching height was achieved using etchant solution of (DI water: H_2SO_4: H_2O_2 = 160 ml: 8 ml: 1 ml) and the sample being immersed in the solution for 23 sec. This process was followed by removal of photo resist using Acetone solution and then measuring the etched profile using surface profiler. The thickness of the etched surface measured was 84 nm uniform through out the Hall Bar sample featuring four arms, compared to 70 nm 2DEG depth and the surface profile as seen at this stage is as shown in figure 1.5
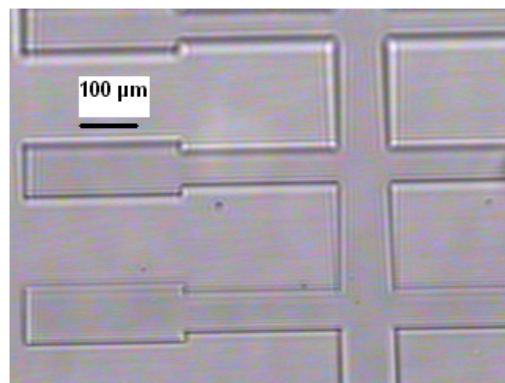
Figure 1.5 Etched surface profile of 2DEG mesa

The data for the etched mesa height achieved for 20 nm, 40 nm, and 60 nm spacer layer samples and the amount of time sample was immersed in the solution for getting the required mesa height is as tabulated in table 1.1

Sample Spacer layer	Concentration of Etchant Solution DI:H2O2:H2SO4	Mesa Height required	Etching Height Achieved	Time for Etching
20 nm	160ml : 8ml :1ml	70 nm	~80 nm	23 sec
40 nm	160ml : 8ml :1ml	90 nm	~100 nm	25 Sec
60 nm	160ml : 8ml :1ml	110 nm	~115 nm	26 sec

Table 1.1 Showing tabulated data of etching height achieved using same etchant solution for different time duration

One of the advantage of wet etching technique is it confines the 2DEG without any kind of contamination and also side wall damage of the mesa formed is less [14] which can ease the continuous run of split gates deposited on Hall Bar as discussed further. As the mesa is formed only thing left now is to form metal contacts at the terminals of Hall Bar.

1.4 Deposition of Metal contacts at the terminals of Hall Bar

The metallic contacts deposited on the Hall Bar terminals should be at the same potential in order to conduct through the mesa easily and to easily measure the potential difference at different points across the Hall Bar and this is achieved by depositing Ohmic contacts at the terminals. Ohmic contacts were also patterned by optical lithography similar to first lithography process carried for mesa formation and Au/Ge/Ni alloy slugs were thermally evaporated for 200 nm metallization. While patterning contacts pads, the mask of the contact pads were aligned to the end of the Hall Bar and the four arms with extremely high accuracy and the pattern developed after exposing the bond pads is as shown in figure 1.6 (a).
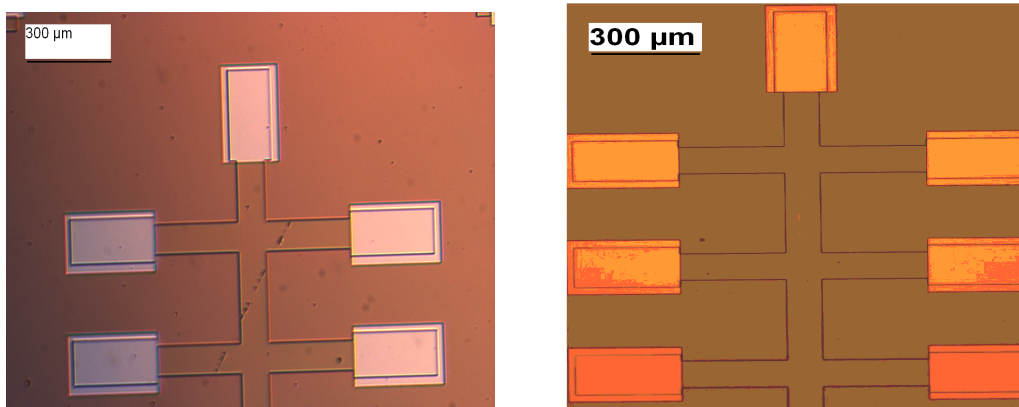
Figure 1.6 Ohmic contacts processing (a) Hall bar pattern after developing ohmic contacts exposure, (b) Hall bar pattern after lift-off process following metallization of Au/Ge/Ni alloy.

While developing the contact pads area exposed, the sample was first immersed in chlorobenzene for 3 min prior to immerse in developer in order to assist lift-off process after metallization. The metallization process using thermal evaporation of the metal alloy, lift-off technique is followed by dipping samples in the acetone for ~2 h and the sample with metal bond pads deposited is shown in figure 1.6 (b).

In order to diffuse the Au/Ge/Ni alloy to contact the 2DEG beneath the surface, Annealing technique was applied at 420 ^{o}C for 90 sec in a reducing ambient such a forming gas (N_2/H_2), which in turn improves the metal-semiconductor contact resistivity.

Finally in the last stage of HEMT fabrication the bond-pads on the Hall bar terminals were bonded on to the chip package using wire bonding. And the samples after this stage were used for Quantum Hall measurements at D.C and A.C frequencies for characterising samples grown at different conditions using MBE.

CHAPTER TWO: CHARACTERIZATION OF HEMT SAMPLES FABRICATED USING QUANTUM HALL MEASUREMENTS

2.1 Introduction

The chapter discusses electronic transport characterization of HEMTs structures fabricated as discussed in chapter one by employing single and variable magnetic fields. The single field quantum hall measurements using conventional Hall bar technique extracts basic information of heterostructured device used such as doping concentration, sheet density, and mobility of the carriers confined in the 2DEG well evaluated from Hall and Longitudinal voltages measured across the Hall bar at required temperature, while the variable magnetic field measurements of HEMTs shows the behaviour of conductivity of electrons in 2DEG getting quantized at particular field values as referenced to well known **Shubnikov-de Haas oscillations,** where the oscillations represents energy spectrum that is made up of 'Landau levels' separated by cyclotron energy as the magnetic field increases the spin-split Landau levels move to higher energy and the period of oscillations increases [15]. That is at particular field values sample acts as complete conductor and at particular field values the sample acts as complete insulator. This technique also gives an idea of oscillation of Fermi-energy through various discrete energy states in which electrons are confined due to 2D confinement at the heterojunction.

2.2 Sample Characterization

Using the above two characterizing techniques, the samples fabricated in MBE with different thickness of AlGaAs spacer layer (20 nm, 40 nm, 60 nm) deposited were characterized using A.C and D.C quantum Hall measurement setup under both Dark and Illuminated conditions, in order to get suitable increase in mobility values with low sheet densities ideally with increase in spacer layer thickness, taking into consideration that there are still enough isolated carriers from ionized impurities to give high mobility values. The data from both A.C and D.C setup analyzed was then compared in order to see the repeatability of the measurements.

Some more samples which were characterized using Hall measurements under similar measurement conditions, where based on variation of Ga % on the tip of Ga gun, varied to 16, 18 and 20 % while growing HEMT structures using MBE machine.

2.3 d.c Quantum Hall Measurements:

This section of the chapter comprises of

- System setup for d.c Hall Measurements
- Data attained using the setup
- Analysis for batch of samples characterized on basis Ga % tip

2.3.1 d.c System setup for Hall Measurements:

(a)   (b)
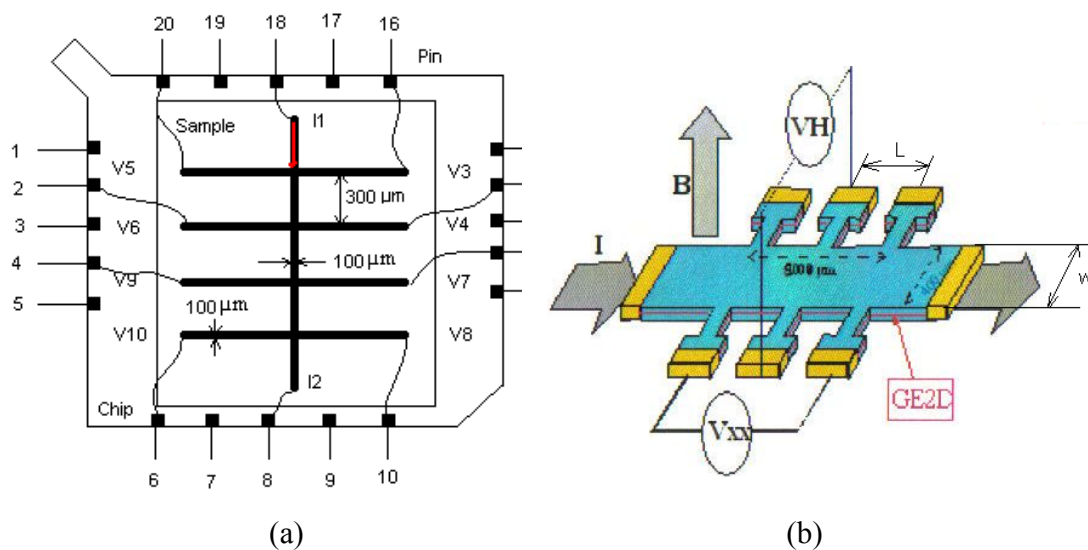
Figure 2.1 Ohmic contacts on HEMTs: (a) pin coordination on chip package used to bond with ohmic contacts, (b) Hall bar measurements setup.

For conducting measurements on Hall bar fabricated, the Hall bar which is formed from semiconductor samples are then bonded on to the chip package in order to make it suitable for handling in Hall measurements as discussed in chapter one, the pin coordination used for bonding and dimensions of the Hall Bar used for measurements are shown in figure 2.1 (a), and the standard Hall bar setup used for d.c measurements is as shown in figure 2.1 (b).

The chip contacts are then connected to various SMU's (Source Measurement Unit) on 'KEITHLEY', where the current was passed through the 2DEG mesa, constant for variable magnetic field and varied for single field measurements from 'KEITHLEY' d.c current source. The sample was suspended via probe as shown in figure 2.2 in direction such that magnetic field was directed perpendicular to the 2DEG channel using Magnet ranging from 0 to 6 T available in Lambda point Refrigerators. Only thing missing on the figure 2.2 is the LED mounted on top of chip carrier in order to excite carrier if the channel was depleted with carriers. Using the four arms in our case pair of voltages was measured, the voltages at the opposite ends of each arm gave Hall Voltage induced due to applied magnetic field while the voltages between the two adjacent arms gave Longitudinal voltages resulting due to the resistance of the mesa between the two arms.
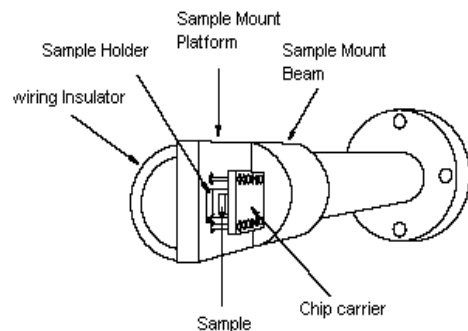
Figure 2.2 Probe used for holding sample

In order to assure the system was working few room temperature measurements were carried out on Hall bar sample, such as applying a current sweep from negative to positive 1 μA without and with applying magnetic field. The I-V curves plotted for these measurements are shown in figure 2.3 (a) and (b) respectively.

Figure 2.3 Room temperature Hall bar measurements (a) in absence of magnetic field, and (b) in presence of magnetic field of 0.2 T

From these results one can see in absence of applied magnetic field the plot of Hall voltage (in red) with current applied across Hall Bar is similar to 'NOISE' (µV) as there is no potential difference induced between the two oppo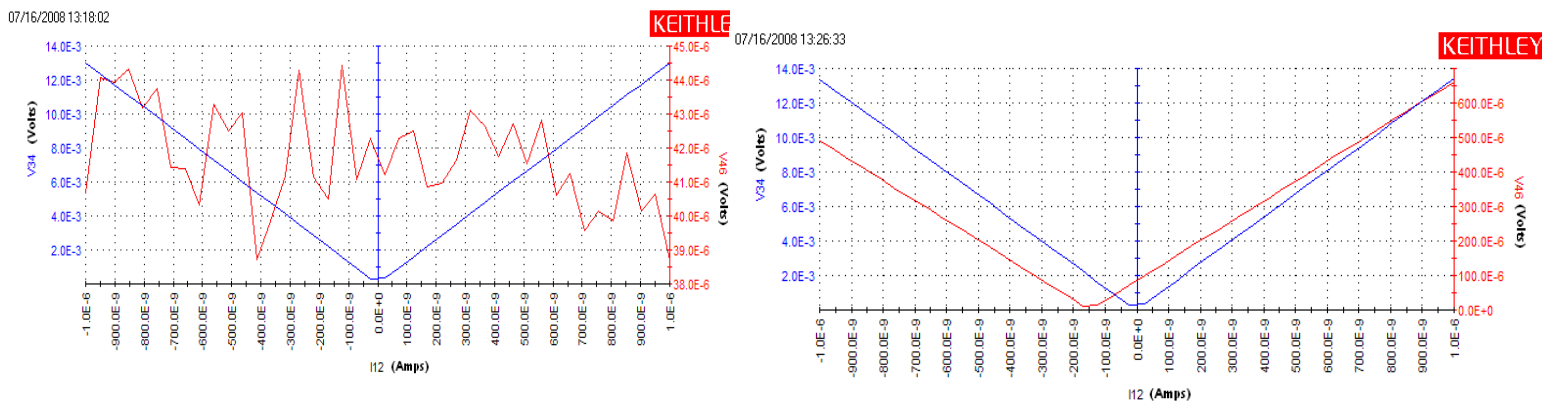site contacts of the each arm while the plot of Longitudinal voltage (in blue) shows the finite resistance plot between two adjacent arms on Hall bar. Whereas even on applying small magnetic field here ~ 0.2 T the potential is readily induced due to force applied on the charges by magnetic field and this is what we expect. Note, all voltages value were taken in magnitude (|volts|) while sweeping current to negative value, also small offset was observed which might be resulting due to sample being not perfectly perpendicular to magnetic field.

2.3.2 Data attained using the setup:

For initial characterization of samples, single field measurements of Hall and Longitudinal voltages across different samples for a constant d.c current were carried out. The current passed through the sample was 1 µA and constant magnetic field directed across the sample was 0.08 T at **1.5 K** temperature. The measurements were taken both under Dark and Illuminated conditions using 'KEITHLEY', the voltages attained were then used to evaluate sample properties such as Sheet Density $[N_s\ (cm^{-2})]$ and Mobility $[\mu\ (cm^2/Vsec)]$ as defined in equation 2.1 and equation 2.2 respectively.

$$[N_s\ (cm^{-2})] = I*B/(q*V_H) \tag{2.1}$$

$$[\mu\ (cm^2/Vsec)] = R_h/\zeta_{2D.} \tag{2.2}$$

R_h being Hall coefficient, is $1/(q* N_s)$ and ζ_{2D} is 2D carrier sheet density between two adjacent/longitudinal contacts in Hall Bar which is defined in equation 2.3.

$$\zeta_{2D} = [R_{xx}*(width,\ w)]/(length,\ L). \tag{2.3}$$

The measurements data achieved for the batch of samples (L 291, L 292, L 293) which were to be characterized on basis of GaAs ratio is discussed first among the measurements taken for characterization of HEMT samples. The description and single field measurement results for the batch of 2DEG samples discussed above are as tabulated below in table 2.1:

Wafer no.	Additional Details	Mobility μ (cm^2/Vsec)		Carrier Sheet Density n_s (cm^{-2})		Sheet Density from SdH n_s (cm^{-2})	
		Dark	Light	Dark	Light	Dark	Light
291	16% Ga1 (40:40:10)	538893.88	743897.95	8.91E+10	1.16E+11	1.26E+11	2.90E+11
		533838.23	701254.03	8.84E+10	1.16E+11		
292	18% Ga1 (40:40:10)	758953.27	1022496.94	5.62E+10	1.75E+11	1.10E+11	2.50E+11
		752066.79	1064763.59	5.62E+10	1.71E+11		
		662741.51	1020996.31	5.65E+10	1.63E+11		
293	20% Ga1 (40:40:10)	312434.27	1325550.71	9.06E+10	1.25E+11	1.30E+11	3.00E+11
		315463.26	1328051.08	9.25E+10	1.22E+11		
		317023.34	1257365.64	9.28E+10	1.23E+11		
		305621.97	1268104.40	9.19E+10	1.26E+11		
		316094.10	1248427.89	9.38E+10	1.27E+11		

Table 2.1 Sheet density values evaluated using single point (0.08 T) and variable magnetic field (0 to 6 T), mobility values evaluated at 0.08 T.

As shown in the table the additional details of samples give information about the Ga % used during growth and the structure of the *Heterojunction* gown from a particular cell in this case Ga 1, from the results evaluated from single field measurements i.e. constant   B (T) as shown in the table, it was observed from all the samples L 292 was giving the highest mobility at 1.5K under dark conditions and also close to highest under illuminated conditions and so was considered to best grown conditions with regards to Ga to As ratio used. Also considerable amount of increase in carrier concentration and mobility values was noted when the sample was **illuminated with led** compared to **dark measurements**. However the sheet densities under Dark conditions for all the samples seems to be really less in terms of 10^{10} (cm^{-2}) which   is pretty lower that what a typically 40 nm spacer sample should have in terms of 10^{11} (cm^{-2}) at this temperature and field values and similarly under Illuminated conditions, and it was proved when the sheet densities for the samples was evaluated from variable field (0 to 6 T) Shubnikov-de Haas oscillation measurements.

In the second part, variable field measurements involved evaluating Shubnikov-de Haas oscillations for each of mentioned samples under magnetic field varied from 0 to 6 T at cryogenic temperatures 1.5 K in Dark and Illuminated conditions, figure 2.4 shows oscillation results for one of the samples characterized (again Hall voltage in red plot and Longitudinal in blue plot) in Dark conditions. Note that x-axis of the plot is in time but this can be easily converted in magnetic field axis, B (T) using the equation 2.4.

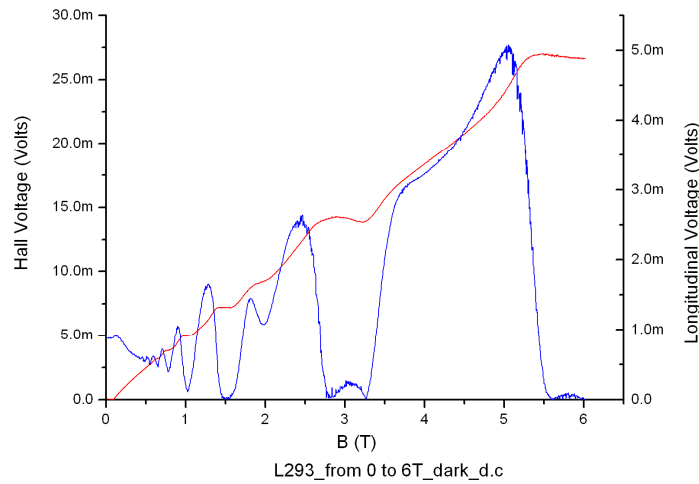B (T) = (0.5*time)/60 T   (2.4)

Figure 2.4 Shubnikov-de Haas oscillations at 1.5 K for L 293

The results from single-field measurements gives a slight skeptical view for evaluating sheet density from single field measurements at lower field values as if there is slight offset in the zero point of magnetic field calibrated for the magnet its impact on the field values near to zero is significantly high than that of at high field values, however it should be noted that field values should not be sufficiently high such that it can result in quantization of resistances.

In case of variable field measurements, sheet density [N_s (cm^{-2})] was evaluated from the equation as defined in equation 2.4

Sheet density = [4.826E10]/Δ(1/B),   (2.4)

Where B is the different values of magnetic field at which longitudinal voltage in the oscillations becomes ZERO and ideally the plot of (1/B) vs P, where P is an integer should be linear passing through the origin, figure 2.5 shows the plot, where SdH oscillations were indexed using an integer P for sample L293 under dark conditions resembling to ideal linear plot. For all of the samples the sheet density evaluated for both dark and illuminated conditions using above analysis is tabulated in table 2.1.
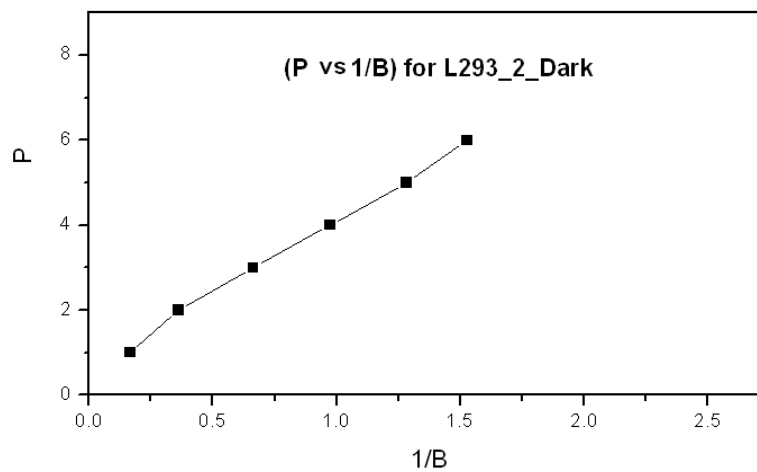

Figure 2.5 variable P vs 1/B

2.4 a.c Hall Measurements:

In this section we will cover aspect of

- Design and Implementation of a.c Hall measurements setup.
- Characterize Hall Bar samples properties measured according to spacer layers.
- Compare the measured properties of samples with the data obtained using d.c setup.
- Analysis of Hall Plateaux occurring in Shubnikov-de Haas oscillations.

2.4.1 a.c Quantum Hall Measurements setup

After finishing d.c Quantum Hall measurements for the last batch of samples which we discussed, decision for converting the existing system in a.c system was made in order to improve the quality of measurements performed and also by using signal recovery Lock-In amplifier for performing measurements instead of 'KEITHLEY' it opens up the limit of current and voltages values we can use for the measurements. For this system we used an a.c signal generator which supplies voltage across the Hall Bar through current limiting resistor and couple of Lock-In amplifiers will be used to read up Hall and Longitudinal voltages from the ohmic contacts on the Hall Bar. The schematic diagram of the a.c quantum hall measurement system is as shown in figure 2.6
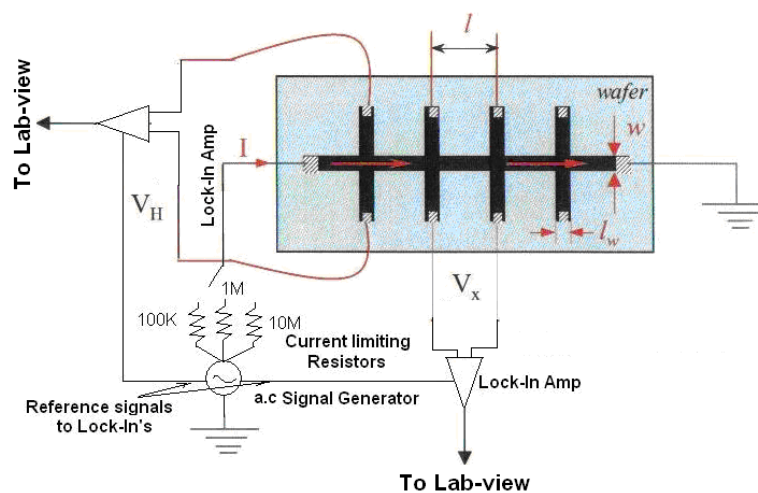

Figure 2.6 a.c Hall measurement setup

After setting up the system, code for interacting Lock-in amps with the signal generator and magnet was developed on Lab-View software which as mentioned earlier was successfully able to control the source signal generator and to read the voltages values from the Lock-In and display it on to the screen however program to control the temperature inside the cryostat still needs some more consideration until then perform a.c hall measurements were performed by manually controlling the magnet and temperature sensors.

2.4.2 Characterization of Hall Bar samples on basis of thickness of spacer layers

One of the main aspects in Quantum Hall measurements is to characterize the ballistic transport of 2DEG affected by thickening of spacer layers giving more isolation to the carriers from the doped ionized impurities as briefly discussed before. And for that reason we used to samples L 270 and L 233 and L 296 grown using identical growth condition in MBE and also by using same growing cell in MBE i.e. GaV in this case, only difference maintained between two samples was the growth of AlGaAs spacer layer which was 20 nm, 40 nm and 60 nm respectively as referring back to HEMT structure shown in figure 1.1. The evaluation of sample properties was carried out in similar way as that of discussed for d.c measurements section (2.3.2) but in order to solve our previous problem of arguably slight offset in the 0 T point, single field measurements with regards to B (T) were now carried at 0.1 T slightly away from 0 T in order to avoid impact of zero offset of the magnetic field, but it was made sure that we didn't go at high enough fields or else the voltages will start getting quantized. And after these evaluations the sample properties evaluated were double checked by analyzing samples through Shubnikov-de Haas oscillations. It was important that the frequency of the voltage applied to the Hall Bar is not in multiples of 50Hz mains as measurement results were easily affected by the mains frequency oscillations. The values of N_s and μ results evaluated from single field measurements, for constant current value of 176.75nA at a.c frequencies in Hall Bar at 1.5K and at 0.1T are as tabulated in table 2.2

QHE MEASUREMENTS AT ~ 1.2K				
Wafer No.	Sample no.	SHEET DENSITY [N_s (cm^{-2})]	MOBILITY [μ (cm^2/V sec)]	Conditions
		by SdH Osc. N_s=(4.826E10)/$\Delta(1/B)$ by LOCK-IN (current I=176.75nA, B=0.1T) N_s=(I*B)/(q*$\bar{V}_H$)	by LOCK-IN (current I=176.75nA, B=0.1T) $\mu = R_{xx}/\zeta_{2D.}$	with info of frequency used in LOCK-IN measurments
L233 40:40:10 with (GaV & Al1)	1	1.70E+11	866666.67	Dark (f = 510Hz)
		1.65E+11 3.39E+11	1648607.59	Light (f = 1.1kHz)
	2	2.75E+11 1.53E+11	875378.21	Dark (f = 510Hz)
		1.52E+11 3.04E+11	1684562.24	Light (f = 1.1kHz)
		2.69E+11		
L 270 20:40:10(GaV-Tip 8% &Al1)]	1	3.01E+11 2.93E+11	815135.14	Dark (f = 721Hz)
		5.09E+11 5.00E+11	1403174.60	Light (f = 721Hz)
	2	3.07E+11 2.99E+11	826492.25	Dark (f = 721Hz)
		5.07E+11 5.05E+11	1423044.32	Light (f = 721Hz)

Table 2.2 a.c Hall Bar measurements, with Sheet density evaluated using single point (0.1 T) and variable field (0 to 6 T) methods, mobility evaluated from single point (0.1 T) method.

Table 2.2 shows the characteristics of the Hall Bar samples evaluated in terms of sheet density and mobility values for L 233 and L 270 from single point field and variable field measurements. First thing to be noted from the tabulated results is the similarities in the sheet density values Ns evaluated from both using equation 2.1, 2.2 and 2.3 and from Shubnikov-de Haas oscillations as shown in figure 2.7 which surely confirmed the skeptical view about the zero offset in zero Tesla value.
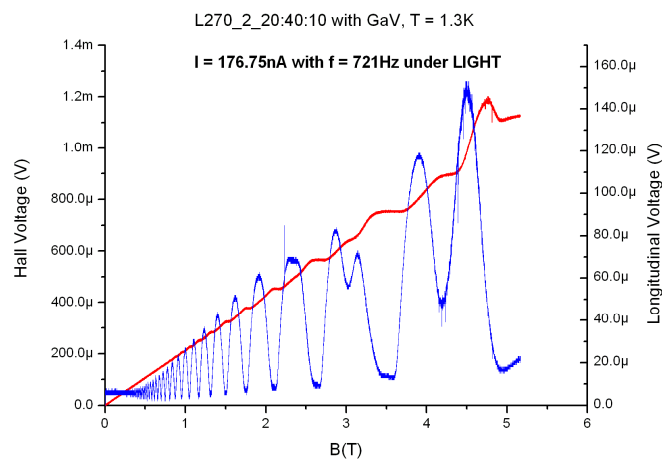
Figure 2.7 Shubnikov-de Haas oscillations evaluated for L 270 under illumination at 1.3 K from 0 to 6 T field, using a.c Hall measurement setup.

The measurements for L 296 were not successful because of the contacts getting frozen up at liquid helium temperatures, it would really interesting to compare the results with rest of the sample batch, nonetheless we can see for L 270, sample with thinner spacer layer has higher N_s and in contrast to L 233, sample with thicker spacer layer having lower N_s both under dark and illuminated conditions as expected thinner the spacer layer more Si electrons will penetrate into the well and so increasing the carrier concentration. Also we can see that notable amount of increase in N_s and so mobility values under illuminated conditions due to electrons moving into lower sub-bands. A clear picture of variation of Sheet density and mobility values for 20 nm and 40 nm spacer samples under dark and light conditions is given by the graphs as shown in figure 2.8 and 2.9 respectively. This is what we expect, as spacer layer increases Mobility increases but the carrier concentration depletes and this trend continues until the there are no enough carriers left to take part in increasing the sample mobility and so it should drop abruptly. This might be the case for us if the AlGaAs spacer layer was increased to 80 or even 100 nm.
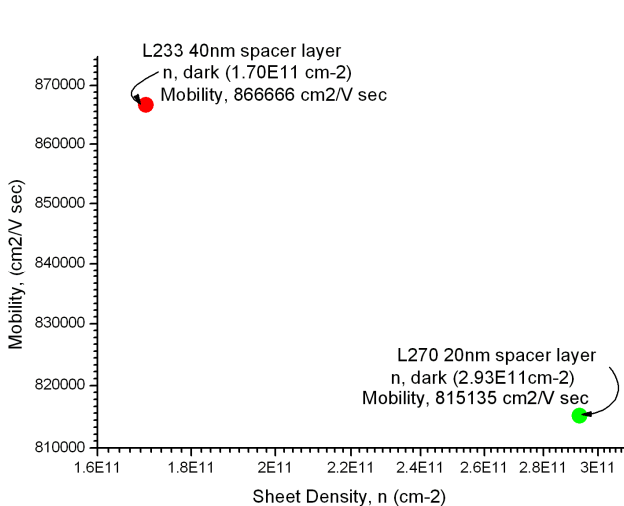
Figure 2.8 Sheet density and mobility comparison for L 233 and L 270 under Dark conditions
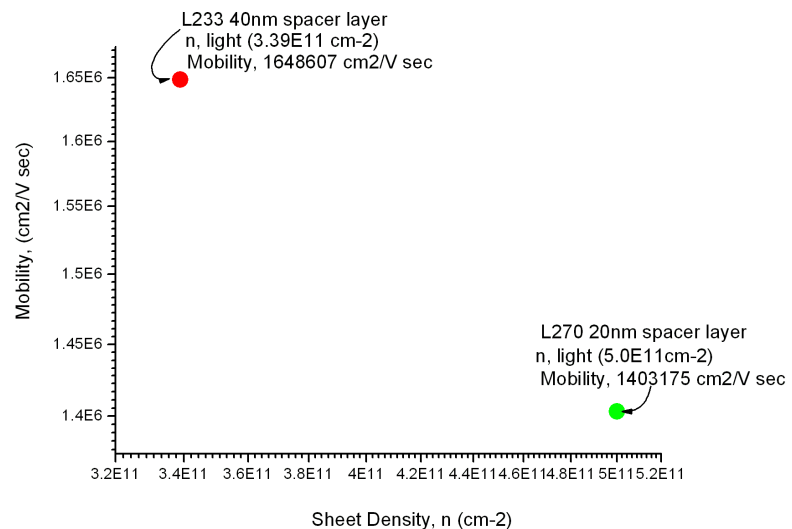
Figure 2.9 Sheet density and mobility comparison for L 233 and L270 under Light conditions

Another way of comparing the characteristics of the two mentioned different spacer layer samples is as shown in figure 2.10, which shows the gradient of the increase in sheet density and mobility due to illumination conditions to that of density in dark conditions for two different spacer layer samples.
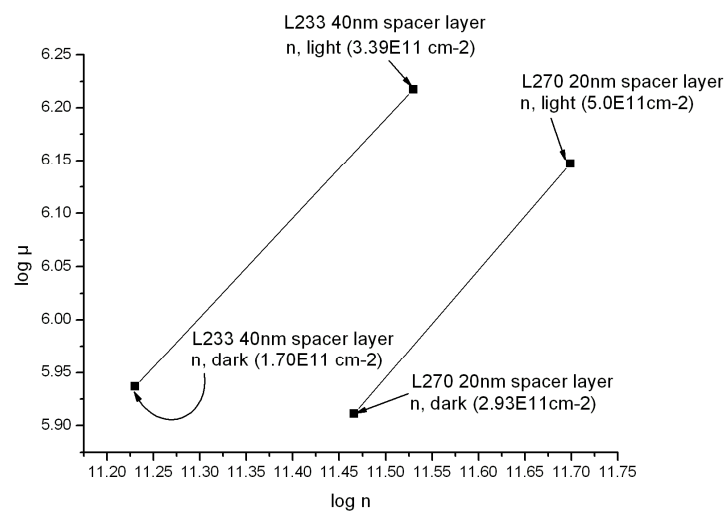

Figure 2.10 Sheet density and Mobility gradient

2.4.3 Comparison of the data evaluated using a.c system to that of measured using d.c system

Single field measurements comparison:

				Carrier Sheet Density n_s (cm^{-2})	Mobility μ (cm^2/Vsec)
270	AC MEASUREMENTS	Dark	f = 721Hz	2.93E+11	815135.14
		Light	f = 721Hz	5.05E+11	1423121.21
	DC MEASUREMENTS	Dark		2.68E+11	1059321.53
		Light		3.51E+11	1312561.52
233	AC MEASUREMENTS	Dark	f = 510Hz	1.70E+11	866666.67
		Light	f = 1.1kHz	3.39E+11	164860759
	DC MEASUREMENTS	Dark		1.50E+11	850787.54
		Light		2.04E+11	1441220.65

Table 2.3 Comparison of Sheet density and mobility values evaluated at 0.1 T with 176.75 nA using a.c Hall Bar setup with that of values evaluated for L 233 and L 270 using d.c setup at 0.08 T with 1 μA.

As we can see from table 2.3, the single point measurements for a.c measurement results were fairly similar to that of previous d.c measurements of the same samples slight offset in values can be seen because the d.c system results were evaluated at 0.08 T while the results calculated using a.c system were noted under effect of 0.1 T magnetic field.

Variable field measurements comparison (0 to 6 T):

With similarities in one point measurements, Shubnikov-de Haas oscillations for the above samples were also reasonably similar under d.c and a.c conditions, and sheet density values evaluated from Shubnikov-de Haas oscillations for a.c setup were very similar to that of measured using d.c setup, e.g. of SdH oscillations comparison for L270 for two setups under light are as shown in figure 2.11 and figure 2.12.
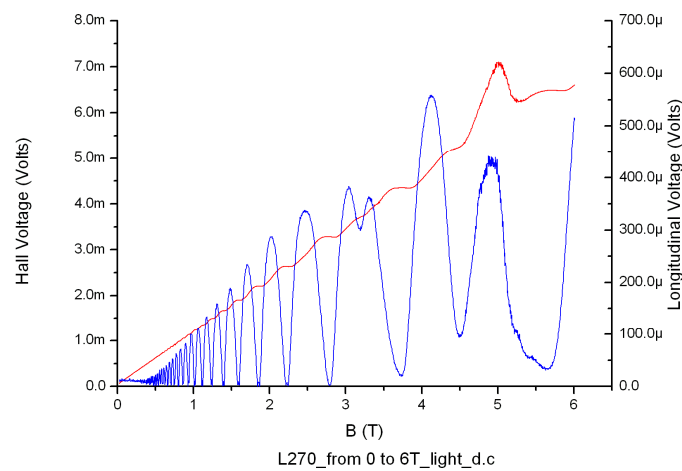

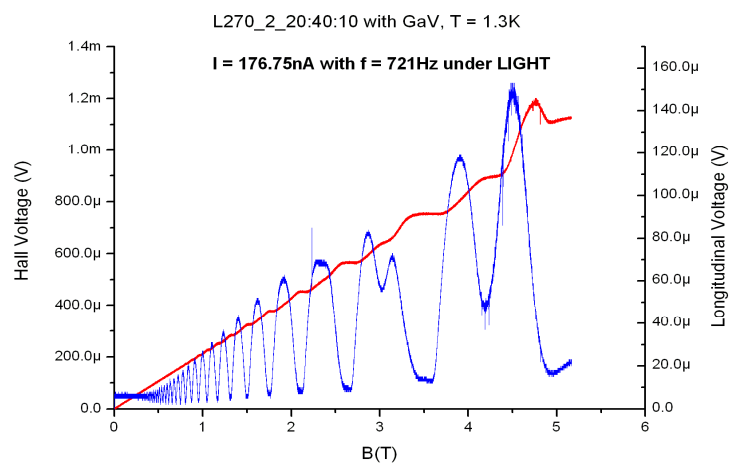**Figure 2.11** Shubnikov-de Haas oscillations for L 270 using d.c setup

Figure 2.12 Shubnikov-de Haas oscillations for L 270 using a.c setup

2.4.4 Analysis of Hall Plateaux occurring in SdH oscillations.

The final part of the analysis includes analyzing the plot of Hall Resistance vs B (T) where the Hall resistance scale is evaluated in terms h/ne^2 which varies in multiples of h/ne^2, so we can accurately determined at what multiples Hall Resistance is quantized between two landau levels. The plots for above samples under both conditions are as shown in figure 2.12 for L 233 and in figure 2.13 for L 270 respectively.

Few comments from the above plots,

As we can see that Plateaus in Hall resistance are occurring at every 1/even multiples (i.e.1/2, 1/4, ..) of h/ne^2 but at high fields they start occurring at every 1/n multiples (n being integer i.e. 1, 2, 3…); this is a result of Zeeman splitting of Landau levels[14]. Also we can see that n which represents completely filled Landau levels, with neB/h electrons under Fermi energy decreases with increasing magnetic field.

With increasing magnetic field we can see the density in each Landau level increases and so to keep the sheet density constant, lower Landau levels will pass through the potential. Due to increase in spacing between these levels it results in oscillation of Fermi-energy with period of 1/B.

In addition note that as we illuminate the sample, the carrier concentration in the sample increases which will increase the number of filled Landau levels inside the Fermi energy as a result we can see from plot of above samples under illumination the multiples of h/ne^2 at which Hall Resistance is quantized are much smaller than that under Dark conditions of same sample at same temperature and so we can say that slope of the Hall resistance plot decreases as the sample is illuminated. From above results we were unable to see quantized hall Plateaux at $1*(h/e^2)$ for having that, we need to go to higher field values than that 6T.
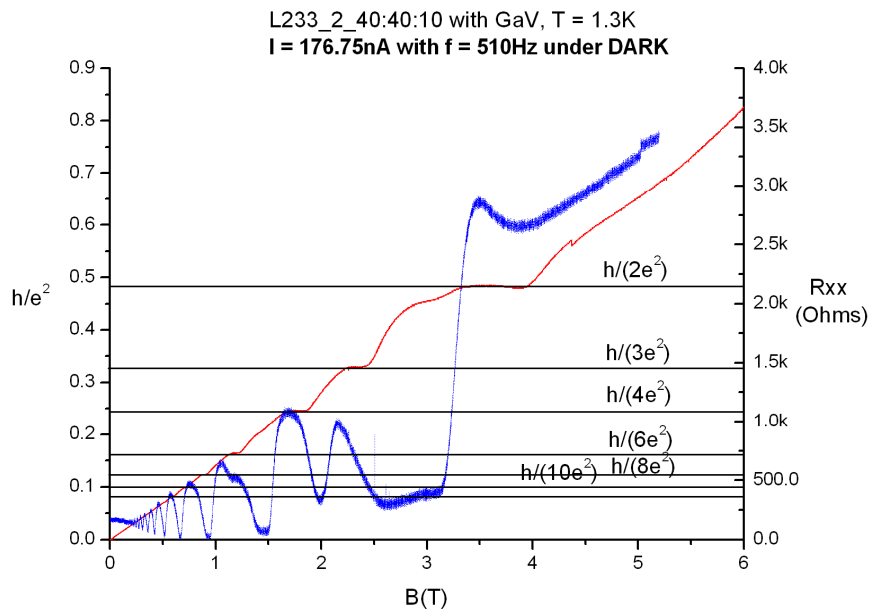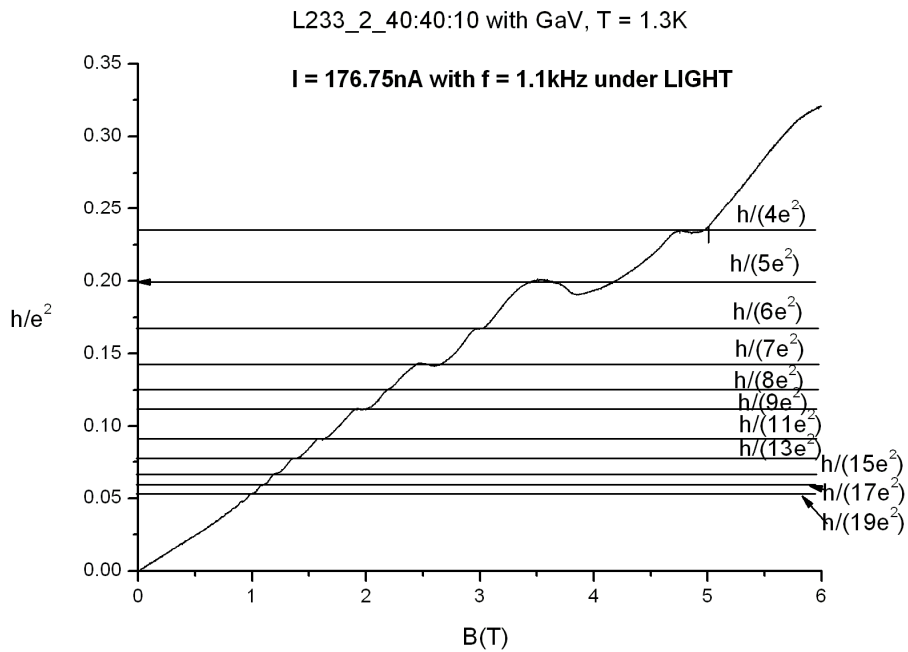
Figure 2.13 Quantized Hall Resistance for L 233 in Dark and Light shown in terms of Plateaux index as function of B (T)
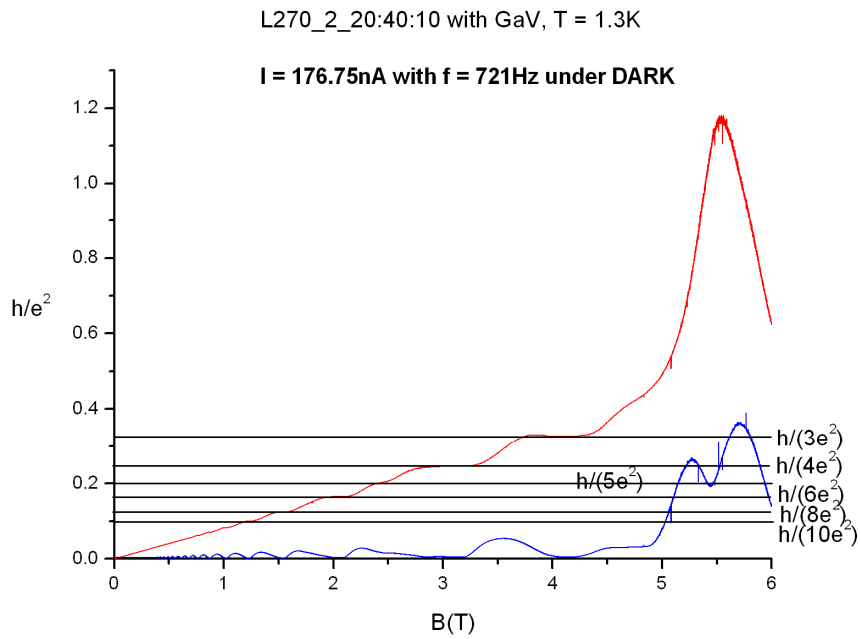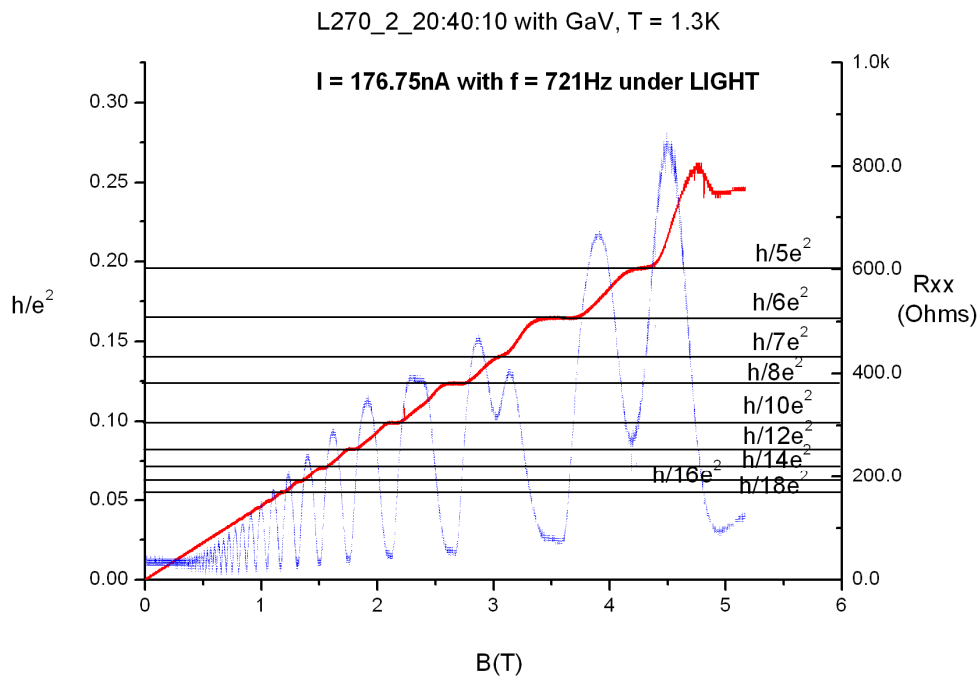
L270_2_20:40:10 with GaV, T = 1.3K

I = 176.75nA with f = 721Hz under DARK

Figure 2.14 Quantized Hall Resistance for L 270 in Dark and Light, shown in terms of Plateaux index as function of B (T).

L270_2_20:40:10 with GaV, T = 1.3K

I = 176.75nA with f = 721Hz under LIGHT

From the comments of above plots it has been observed that for a 2DEG, the resistance is quantized at every 1/even multiples (i.e.1/2, 1/4, ..) of h/ne^2 at low magnetic field values and then finally the plateaus occur at every 1/integer multiples at high magnetic field values. However this is not the case when the electrons in the 2DEG layer are undergoing parallel conduction [23]. As one can see from figure 2.15, for L 233 (40 nm spacer) structure, when the carriers were excited using illumination it resulted into conduction of carriers through a parallel channel as observed by quantum transport measurements. One of the important properties of parallel channel conduction is that, in the SdH oscillations observed the oscillations of the longitudinal voltage will not go back to zero point and as a result the quantized resistance plateaus doest not essentially occur at the above predicted values under low and high magnetic field instead it will occur at random multiples. And this is the case which explains the plot of quantized resistance plateaus for L 233 under illumination conditions as shown in figure 2.13.

Note the plot was not in format of data so wasn't shown from 0 to 6 T but instead shown from 6 to 0T.
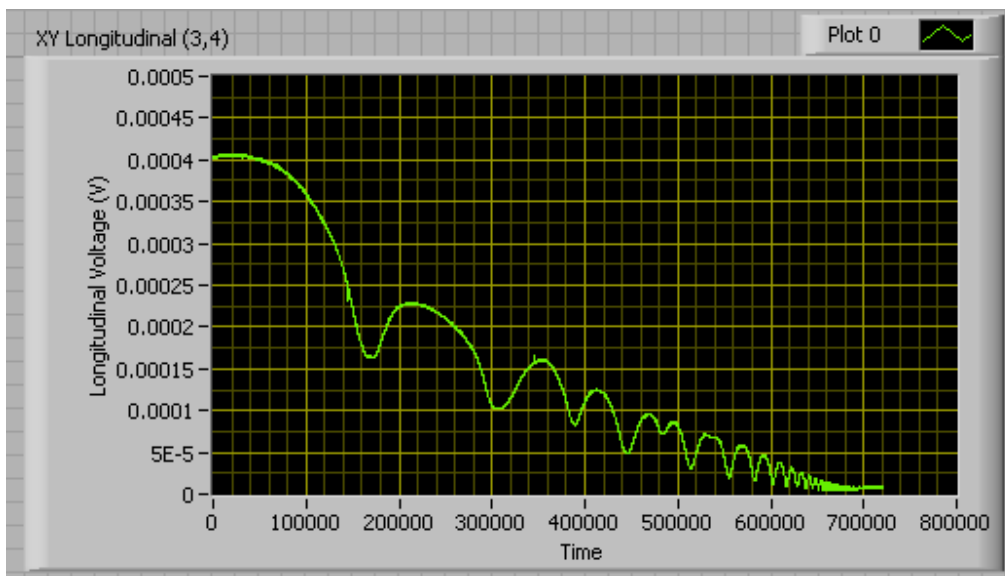

Figure 2.15 Quantized longitudinal voltage plotted for parallel conduction phenomena of 2DEG carriers.

CHAPTER THREE: FABRICATION OF 1D ELECTRON TRANSPORT DEVICES IMPLEMENTING METALLIC SPLIT-GATES

3.1 Introduction

Fabrication of Split-gate devices is carried out in similar way as in conventional HEMT fabrication method up to a point where the Ohmic contacts are diffused to make contact with the underlying 2DEG layer; this gives a chance to exploit the high performance of 1D channel devices using reliable and low-cost fabrication technique. The fabrication process afterward involves drawing pattern of split-gates on the Hall bar mesa using Electron Beam Lithography (EBL), because the pattern by this method is time-consuming it is familiarly used to pattern small areas where the highest resolution is required as in this case defining fine features of split-gates. Most important aspect of patterning these devices is the width of the quasi one-dimensional channel defined by the split-gates as the quantum corrections in conductivity becomes one dimensional only when the phase relaxation length of an electron and the interaction length are greater than the channel width defined [16-20]. After working out the above requirement from the 2DEG mobility values of the sample to be used, channel width of 300 nm was defined by the split-gates deposited on Hall bar using EBL. A conceptual example of 1D ballistic transport defined by split-gate devices is shown in figure 3.1.
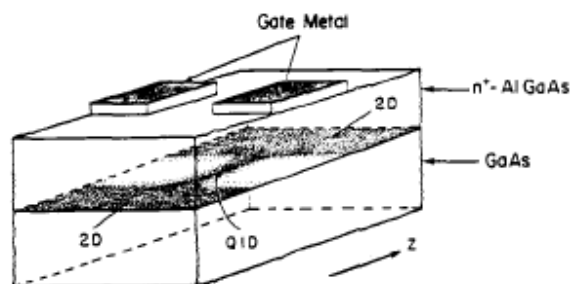

Figure 3.1 Visual Illustration of quasi-1D channel defined implementing split-gates

3.2 Fabrication of 1D channel device and split-gates patterning

The 2DEG samples which was used for patterning split-gates on were AlGaAs/GaAs heterostructures grown in MBE machine the layers from bottom to top are GaAs substrate, GaAs buffer, an undoped AlGaAs spacer (s = 20 nm), a Si-doped AlGaAs layer (d = 40 nm), an undoped GaAs cap (c = 10 nm), respectively as referenced in figure 1.1. Processing of these samples was carried out as explained in chapter 1, the Hall bar mesa of 80 nm was developed using optical lithography and wet etching process. Also same as before Ohmic contacts were deposited with high accuracy at the terminals using conventional thermal evaporation process of Au/Ge/Ni alloy. After annealing, Hall bar sample was ready for deposition of split gates.

However the question was whether to draw bond pads for the split gates first or to pattern the split gates itself. The answer to this question was the method which can give continuous over run of the split-gates at the mesa edge can be used. A visual pictures for the above two conditions discussed, depositing bond-pads first or patterning and depositing split-gates first are as shown in figure 3.2 (a) and figure 3.2 (b) respectively.
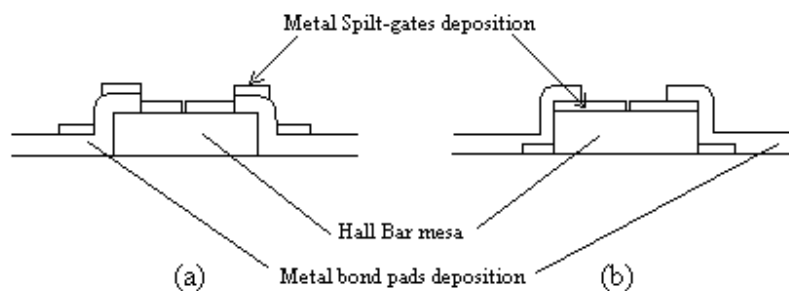

Figure 3.2 TEM view of pattern formed by split-gates and metal deposition on Hall Bar mesa (a) metal Bond-pads deposited first, (b) split-gates deposited first.

As one can see from figure 3.2 (a), while depositing the bond pads for the gates first can result in discontinuity for the over run of the split-gates at the mesa edges, because thickness of the metal need to be deposited for the split-gates is nearly half to that of metal thickness needed for bond pads. This break in the connection from gates to the contacts can result in hysteresis effect of the pinch-off voltage needed to deplete the channel, i.e. by increasing the negative bias applied to the gates, the pinch-off voltage noted to close the 1D channel will be different to the voltage noted by decreasing the negative bias applied in order to open the channel. However this problem can be prevented by patterning and depositing metal on split-gates prior to forming bond pads as shown in figure 3.2 (b) because it can give continuous connection from gates to the pads.

In order to write split-gates pattern on the Hall bar e-beam lithography was performed using Raith-50 e-beam writer. This time instead of forming a layer of Shipley photo resist on the sample, a polymethylmethacrylate (PMMA) bilayer (495 A4) was used as a spin coated resist which was spun at 5000 rpm for 30 sec giving film thickness deposited on Hall bar of around 1800 A^o which was similar to what was expected from the manufacturer datasheet as attached in **appendix A**. The resist coated sample was then baked at 170 ^{o}C for approximately $\sim$ 2 hours.

E-beam lithography was then performed to write the pattern of split-gates on the Hall bar mesa, all together four pairs of gates were to be formed on the Hall bar sample. While performing this technique extreme care was taken in setting up dose parameters and exposure time for the e-beam. As to get good exposure, these parameters should be precisely in accordance with the resist thickness deposited onto the sample; any un-uniformity in the resist thickness can result into poor exposure of the area to be patterned and can eventually result into poor metallization of gates, which was the case observed for one of the samples and poor metallization result is as shown in figure 3.3.
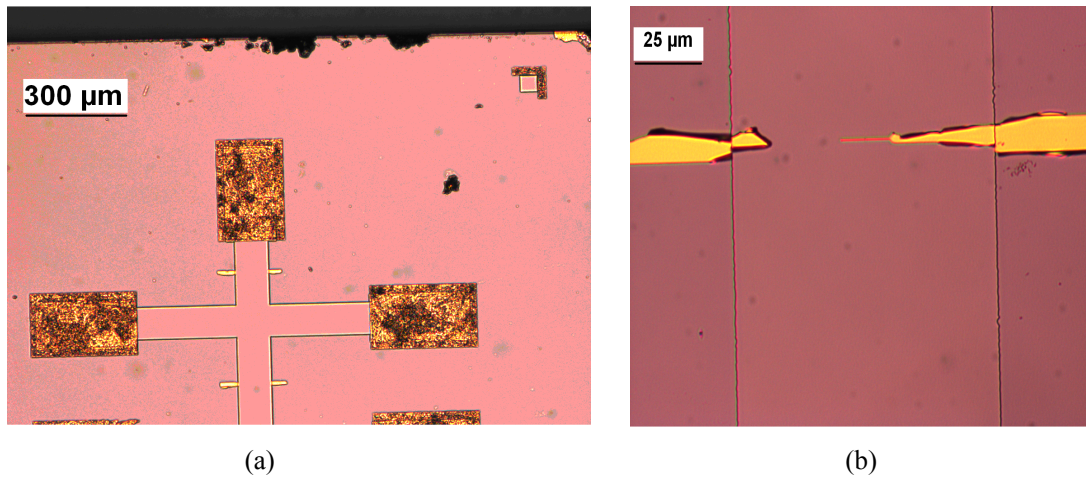
| (a) | (b) |

Figure 3.3 Poor deposition of metal on split-gates because of the unsuccessful exposure resulting from the set dose parameters not in accordance with PMMA resist thickness (a) All gates broken at the edge of mesa, (b) magnification of the damage on individual gate.

After performing e-beam lithography the pattern written on the sample was then developed using standard PMMA developer solution of MIBK:IPA (1:3) for 70 sec and then sample was rinsed in IPA for 30 sec. The spilt gates pattern with split width of 300 nm was successfully developed and is as shown in figure 3.4
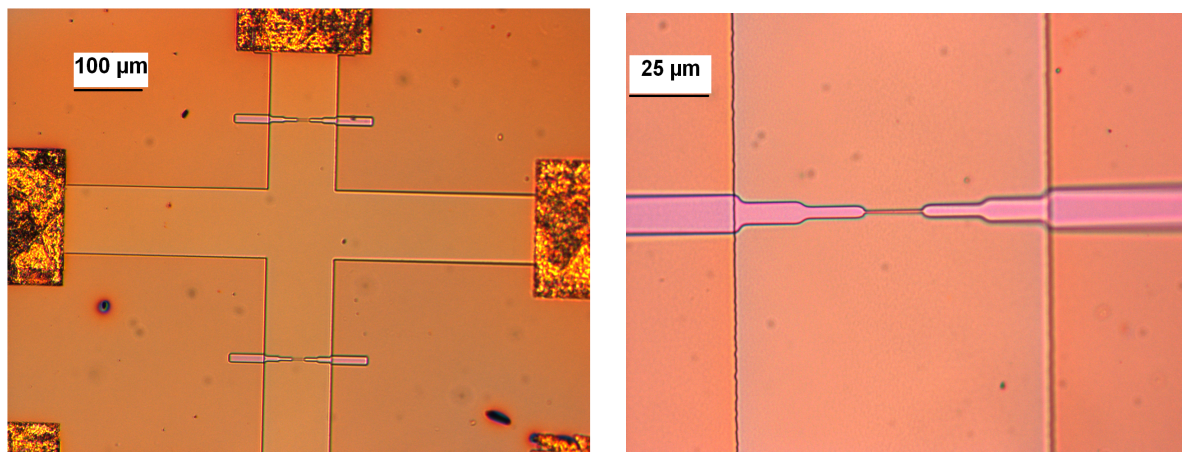

Figure 3.4 Successfully developed e-beam lithography from Hall Bar view and individual split-gate view.

After developing the lithography carried out on the sample metal was deposited on the split-gates in order to make contacts with the bond-pads and so with negative bias source.

The contacts formed at this stage are Schottky contacts in order to restrict bidirectional flow of electrons to prevent any leakage in negative bias applied to the gates.

The metallization carried out consisted of thermal evaporation of 20 nm of Ti in order to provide better adhesion to the GaAs surface followed by 60 nm Au. Au was chosen for the metallization process because of the reproducible Schottky barrier which forms at the semiconductor interface. Thickness of Au was evaluated from the rule of thumb for PMMA resist, where the thickness of the metal deposited should be around one-third of the resist thickness (1800 A^o) spread for e-beam lithography. And the lift-off process during this stage will be same as previously discussed; only thing to note is for successful lift-off the amount of time sample was immersed in acetone was longer around ~8-10 hours because of the small feature area patterned.

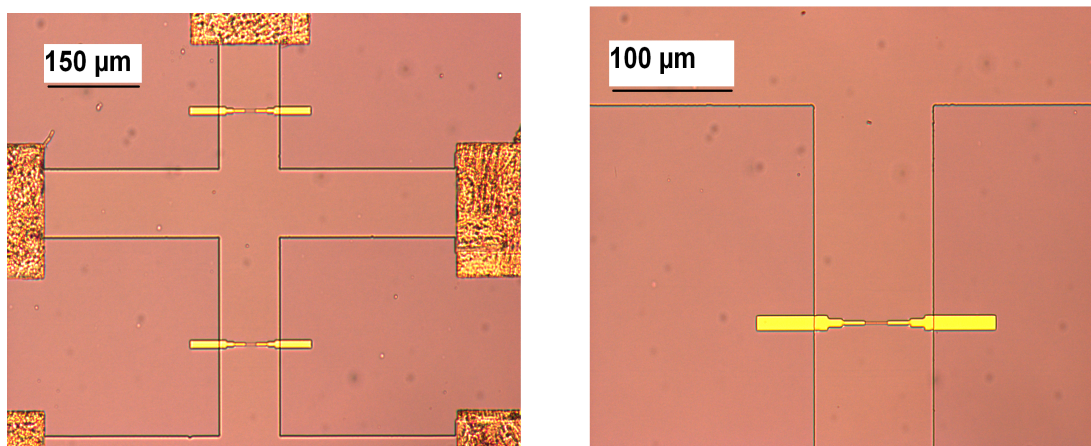The metallic gates on the sample after this phase as observed are shown in figure 3.5

Figure 3.5 Successfully lift-off after metallization process of Ti/Au (20 nm/60 nm) on split-gates developed using e-beam lithography from Hall Bar view and individual split-gate view.

The bonding pads with larger feature area were then drawn by time-efficient conventional optical lithography process which were then developed as mentioned in section 1.4 and the process was then followed by metallization of the pads again to make sure that the contact formed between gates and pads was leakage free, Schottky contacts were developed using thermal evaporation of 20 nm of Ti followed by thicker layer of 100 nm Au.

At the final stage of fabrication process for split-gates devices the bonding pads were bonded onto the chip package before bonding the gates to the contacts on the package, all of the contacts on package were shorted with bonding wires using 'stitch bonding technique' in order to prevent any generation of unnecessary charge at gates which can damage the split-gates devices. The metallic pads on the sample connecting with gates before bonding them to the package are as shown in figure 3.6
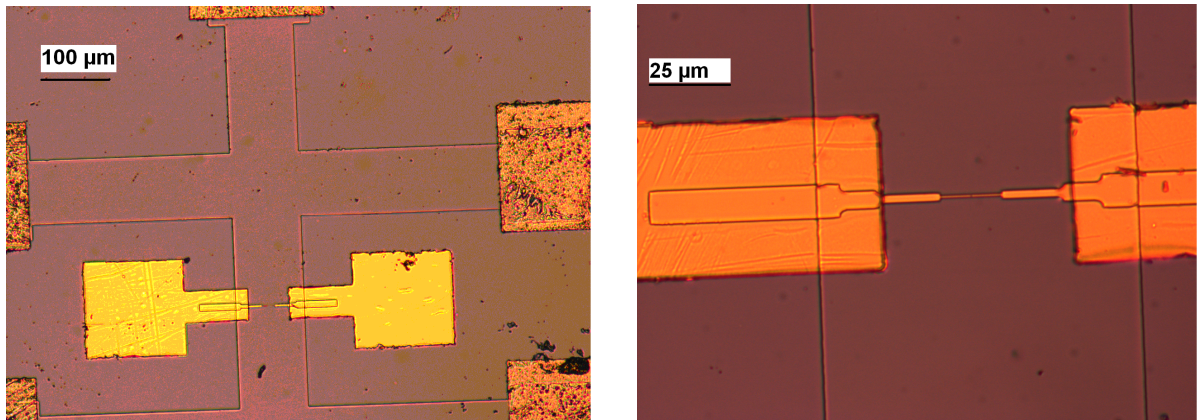

Figure 3.6 Successfully lift-off after metallization process of Ti/Au (20 nm/100 nm) on bond pads developed using optical lithography from Hall Bar view and individual split-gate view.

CHAPTER FOUR: REALIZATION OF QUASI-ONE DIMENTIONAL CHANNEL USING SPLIT-GATE DEVICE

4.1 Introduction

The split-gate devices used are essentially HEMTs with high mobility values attained, having a narrow slit in the gate deposited on the cap surface, underneath which 2DEG is formed [21]. On applying negative gate voltage, gates start depleting the 2D electron gas formed underneath the cap layer, thereby reducing the width of the channel. This results in complete collision free ballistic transport for the electrons. The main aspects for the ballistic transport is that the electron wavelength (~ 500 A^o) should be comparable to the width of the channel defined in our case (300 nm), which means that the electron phase coherence length (= 8.5 μm) exceeds the width of the channel [22]. Hence by using split-sates as point contacts, electrostatic depletion of 2DEG underneath the gate occurs which will result in transformation of classical electron transport to quantum ballistic transport.

4.2 Previous Research work

From the previous research work being done on analyzing Quantized conductance of split-gates devices [22]; the point contacts were developed on a 2DEG structure, where the sheet density of the material was 3.56E11 (cm^{-2}) and the mobility gained by the doped carriers was 850,000 (cm^2/Vsec) at 0.6 K. The split-gate with an opening of 250 nm wide was deposited such that it fulfilled all the requirements for quasi-one dimensional transport and it is as shown in figure 4.1.
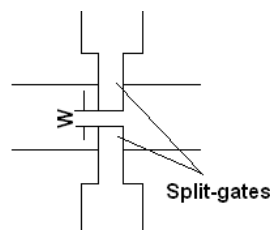

Figure 4.1 Shows width of channel defined using Split gates

In order to define the channel, voltage was applied to the 2DEG Hall bar which was kept below a point at which it starts electron overheating. As negative bias was applied across the gates and increased, the channel started depleting the electron carriers until the pinch-off condition occurred. It was observed that the channel depletion occurred at V_g = -0.6 V and the 2DEG layer underneath at this bias value was depleted. By further decrease of gate bias the width of the channel defined was gradually reduced until the channel pinch-off occurred at V_g = -2.2 V. The resistance of the point contacts was measured and after its conversion in to conduction plot, it was plotted with respect to that of gate voltage applied. The plot of gate bias depleting the channel is shown in figure 4.2 (a), while the plot of conduction steps noted from the point when channel was depleted to the point where channel was pinched-off is as shown in figure 4.2 (b).
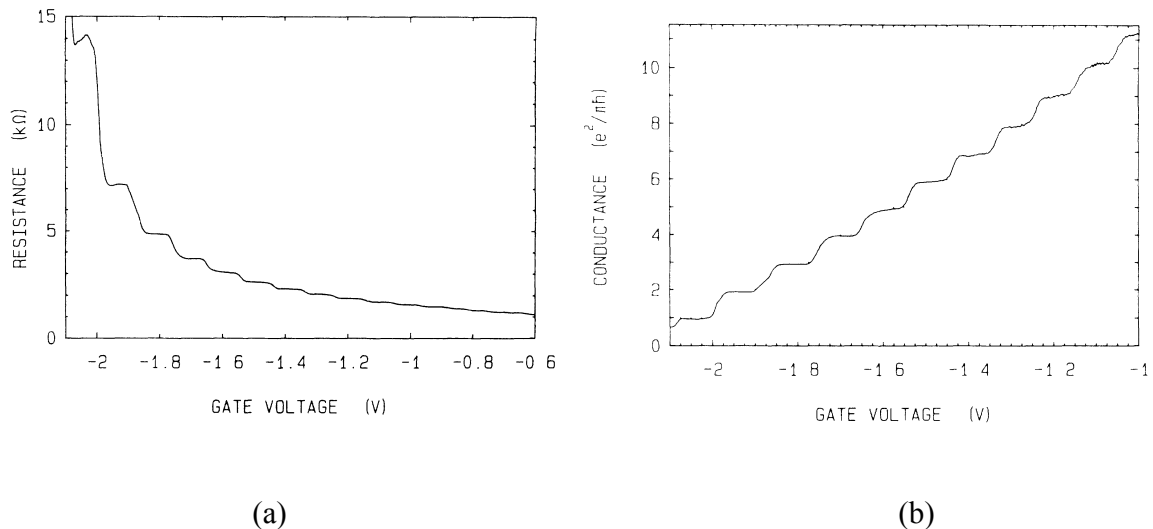

(a)   (b)

Figure 4.2 Quantized transport gained by negative gate bias applied, (a) point contact resistance vs gate voltage, (b) point contact conductance vs gate voltage, quantized at every integer multiple values of $e^2/\prod h$.

Note that while plotting the quantized conductance the lead resistance was subtracted and quantized conductance for ballistic transport was evaluated in terms of multiple values of $e^2/\prod h$.

In further study of the experiment, analysis was carried out on number of plateaus that were observed from the channel depletion to its pinch-off and its relation to the maximum value of width of the channel defined lithographically. And relation of the gate width variation (i.e. channel width) to the applied gate voltage.

4.3 Practical realization of the 1D split-gate devices experiments

In order to follow footsteps of the previous research work carried out on conductance measurement of 1D split-gate devices, the point contacts as discussed in chapter three were deposited on a 2DEG structure (L 270) of which sheet density measured is 2.93E11 (cm^{-2}) and mobility 815135.14 $(cm^2/Vsec)$. After bonding 300 nm wide gap split-gate devices onto the chip package, setup for measurement was analyzed. The final setup designed for quasi-1D channel measurements is as shown in figure 4.3.
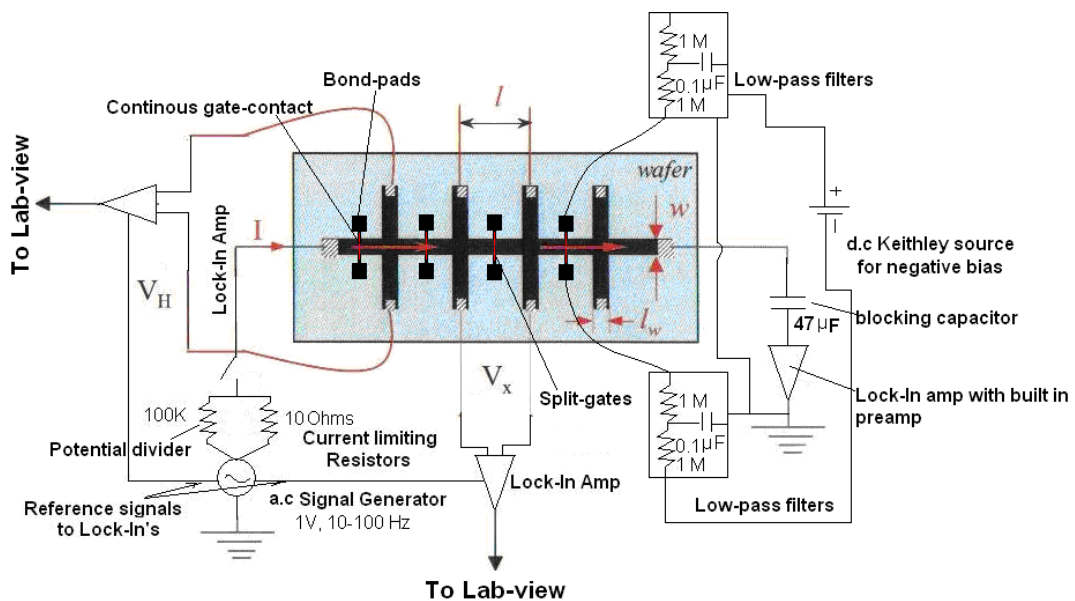

Figure 4.3 Final setup designed for quasi-1D transport measurements

In order to observe quantized conductance across the quasi-1D channel formed, 100 µV was applied across the Hall bar through potential divider circuit and the current from the other end of the hall bar was noted in order to see the channel effect on the flowing carriers. Hence when negative bias was applied across one of the four gates through low-pass filter it results into carrier depletion underneath the gate and this will limit the amount of current coming out on the other end of Hall bar. The channel depletion results, when negative bias up to 3 V applied to a split-gate is as shown in figure 4.4.
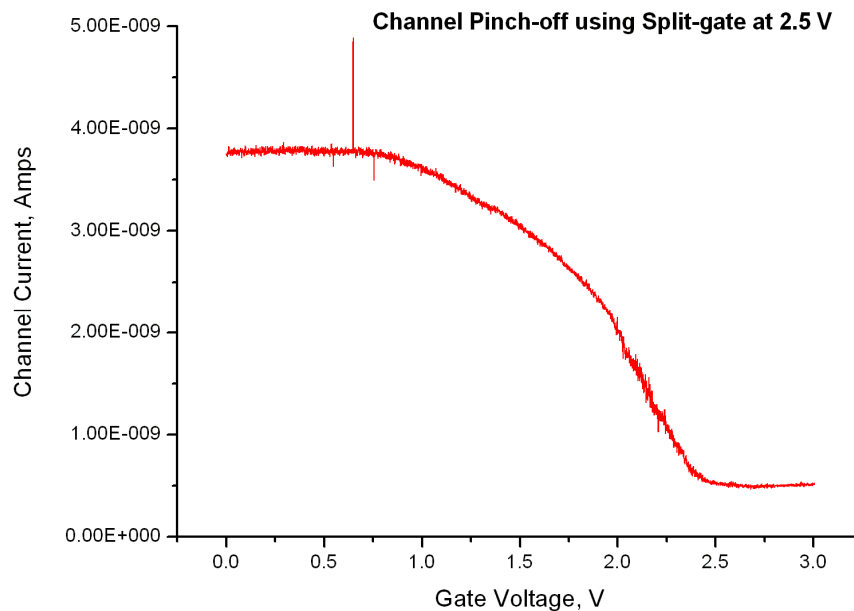

Figure 4.4 plot of gate voltage vs channel current

As seen from the figure, the channel starts to deplete at gate bias of 0.1 V however further decrease in gate bias leads to channel pinch-off at around 2.5 V. These measurements were performed at 1.5 K, and this might be one reason for absence of conductance steps expected with respect to gate voltage. The reproducibility of the channel pinch-off was really good as well which gives positive indication for continuous overrun of split-gates on the mesa.

CONCLUSION

The report gives an overview of fabrication and semiconductor processing methods used to make low-dimensional nanostructures, with a detail description of the electron transport process seen in these low-dimensional structures. In particular, we have seen how the growth parameters can be exploited in order to minimize impurities scattering. The initial part of the report discusses the procedure of a HEMT processing used to develop 2D channel devices, and how this was extended for the development of 1D channel devices (i.e. optical lithography, etching and metallization). Whilst characterizing quantum transport in these 2D channel devices the samples were divided in two batches. For the first batch of HEMT samples, characterization was carried out in order to investigate amount of GaAs ratio used in Ga-1 cell of MBE which can give highest mobility of carriers in the 2DEG formed at the heterojunction. From the measurements, it has been concluded that samples fabricated using 18 % Ga for GaAs ratio produce the best performance. With the second batch of HEMT samples, characterization was carried out on the basis of the thickness of AlGaAs undoped spacer layer; this spacer layer was varied to give high mobility of carriers in the 2DEG layer. The samples with different spacer layers that were analyzed were 20 nm and 40 nm spacer layer. It was observed from the measurements as expected, that narrow spacer layer samples gave higher sheet density values than that of a thicker spacer layer samples but a lower mobility. It was also noted that the trend in spacer layer analysis results were similar for both under dark and light conditions.

The report also discussed the fabrication and measurements of quasi-one dimensional systems, its fabrication process and the quantum transport in these systems. A complete process of pattering point-contacts was carried out in a class-100 clean room (same as that for HEMT processing) starting from optical pattering of Hall bars followed by patterning the split-gate devices using (EBL) to the metallization process for adding bond pads to connect to the e-beam defined gates. These devices were tested at 1.2 K; by applying a negative bias across the gates, channel depletion and pinch-off were observed. However, clear quantized conductance steps were not clearly visible, possible owing to the elevated temperature of the measurements.

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APPENDIX A: DATASHEETS

A.1 MICROPOSIT S1813 PHOTORESIST

A.2 MICROCHEM PMMA RESIST