Ultra-scaled MoS_2 transistors and circuits fabricated without nanolithography

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Supporting Information

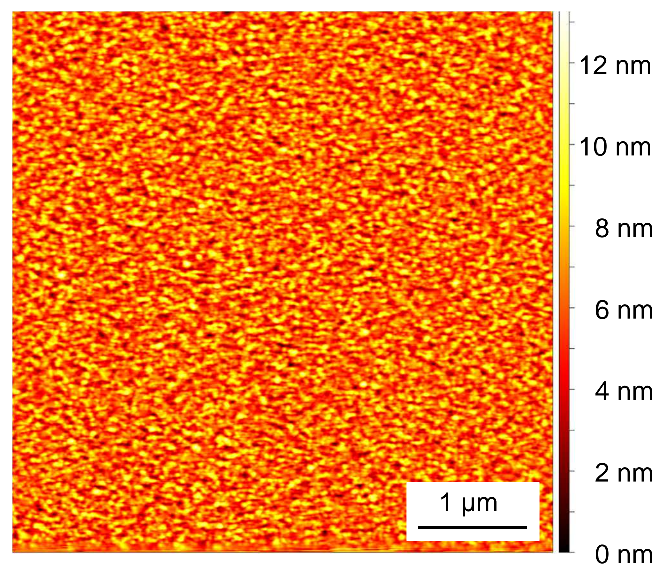

Figure S1. An AFM image of an Al/AlO_x gate stack. The stack was obtained by evaporating Al on an SiO_2 substrate. The surface roughness (RMS) is 1.52 nm.

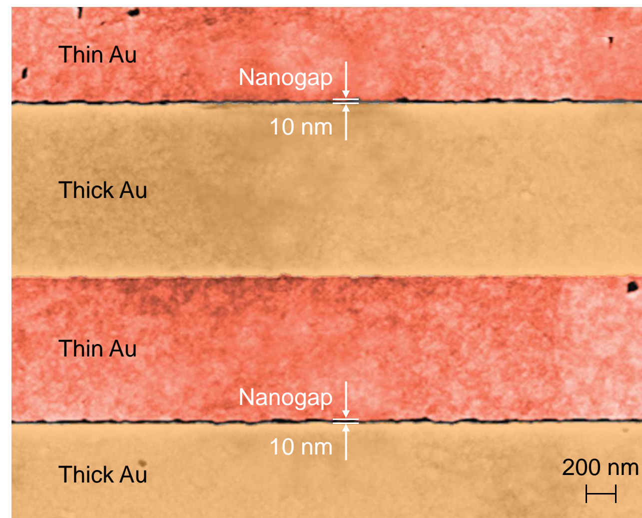

Figure S2. A large area scanning electron microscopy (SEM) image (in false colors) of two nanogaps. The initial Au source and drain contacts (yellow) were fabricated with a resolution of ~ 1 μm. The nanogaps were created by evaporating a thin layer of Au (red) under an angle of 15° with respect to the perpendicular axis of the sample/image (inclined towards the bottom part of the image).

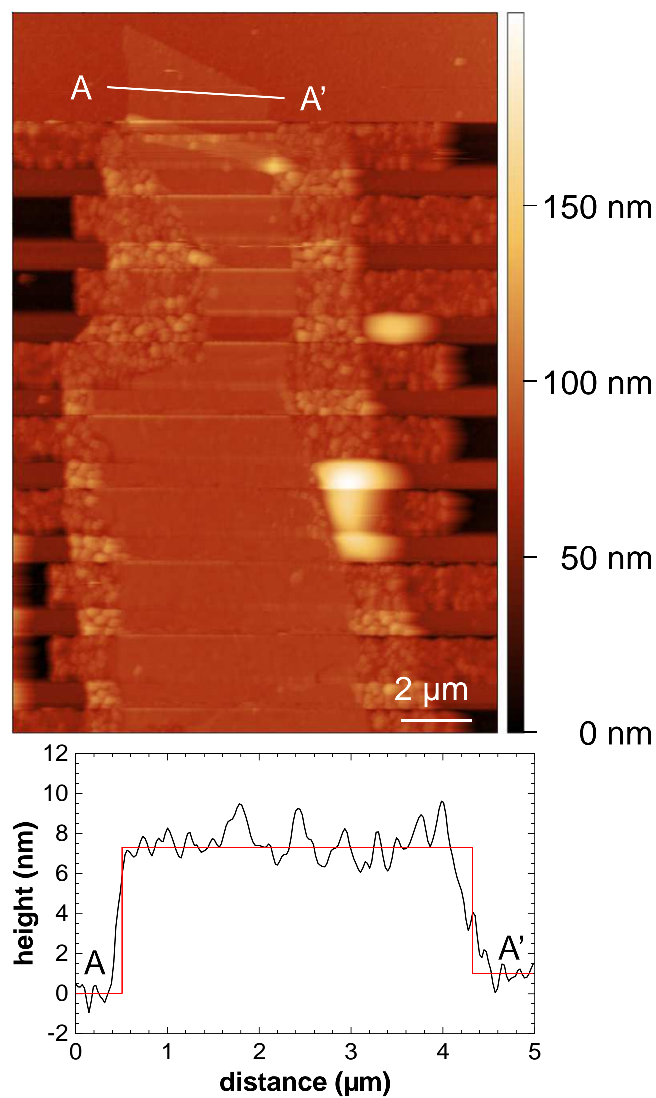

Figure S3. An AFM image of several exfoliated MoS_2 FETs, out of which one is from Fig. 2. The height profile along the section A-A' is shown below the image. The section is taken across the MoS_2 flake and the height is calculated with respect to point A.

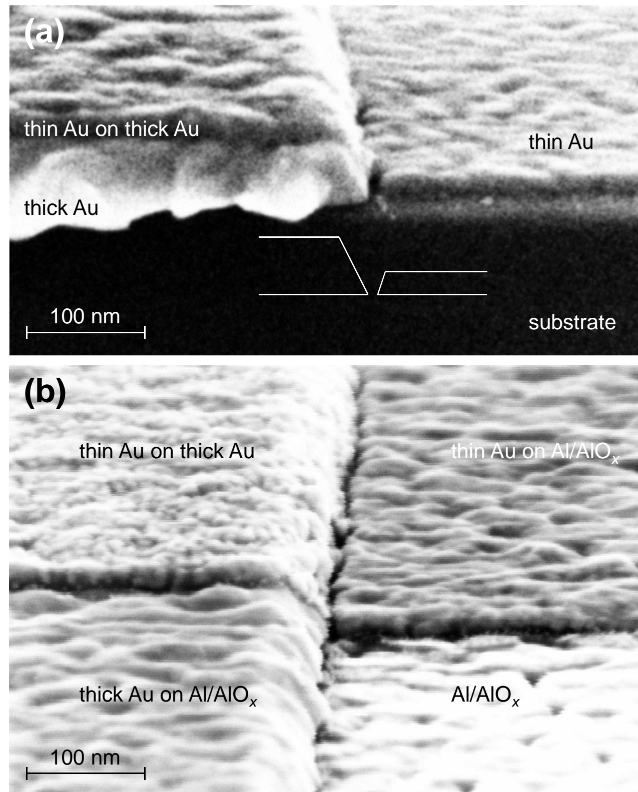

Figure S4. Tilted SEM images of a gap between the source (thick Au) and drain (thin Au). (a) Tilted image of the gap reveals oblique sidewalls of the contacts, as sketched in the inset. Such sidewalls are a consequence of the directional metal deposition by e-beam evaporation used to create the contacts. The thick contacts are obtained by depositing metal through a developed part of a resist, which initially creates vertical sidewalls of the contacts. However, as the deposition of the metal continues, the metal deposited at the top part of the resist tends to laterally expand [1, 2] thereby reducing the effective size of the opening in the resist. Consequently, the width of the contacts reduces with height, creating oblique profile observed in the thick contacts. Similarly, the shadow evaporation leads to the oblique profile of the thin contacts due to the deposition of the metal on top of the thick contacts (although this is not pronounced due to the small thickness of the thin contacts). Therefore, the actual gate length is probably slightly shorter compared to what was observed in the standard (top-view) SEM images shown in the main text. (b) Tilted SEM image showing the local Al/AlO$_x$ back gate (bottom right), thick contact (left), and thin contact (upper right).

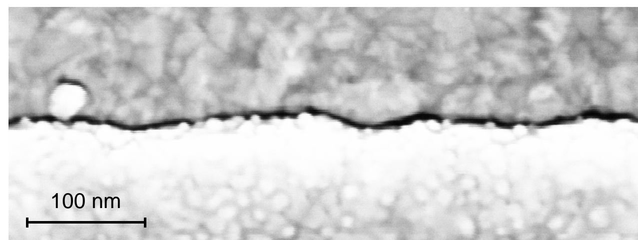

Figure S5. SEM image of a very narrow gap (5 nm) which cannot be cleared by thermal annealing.

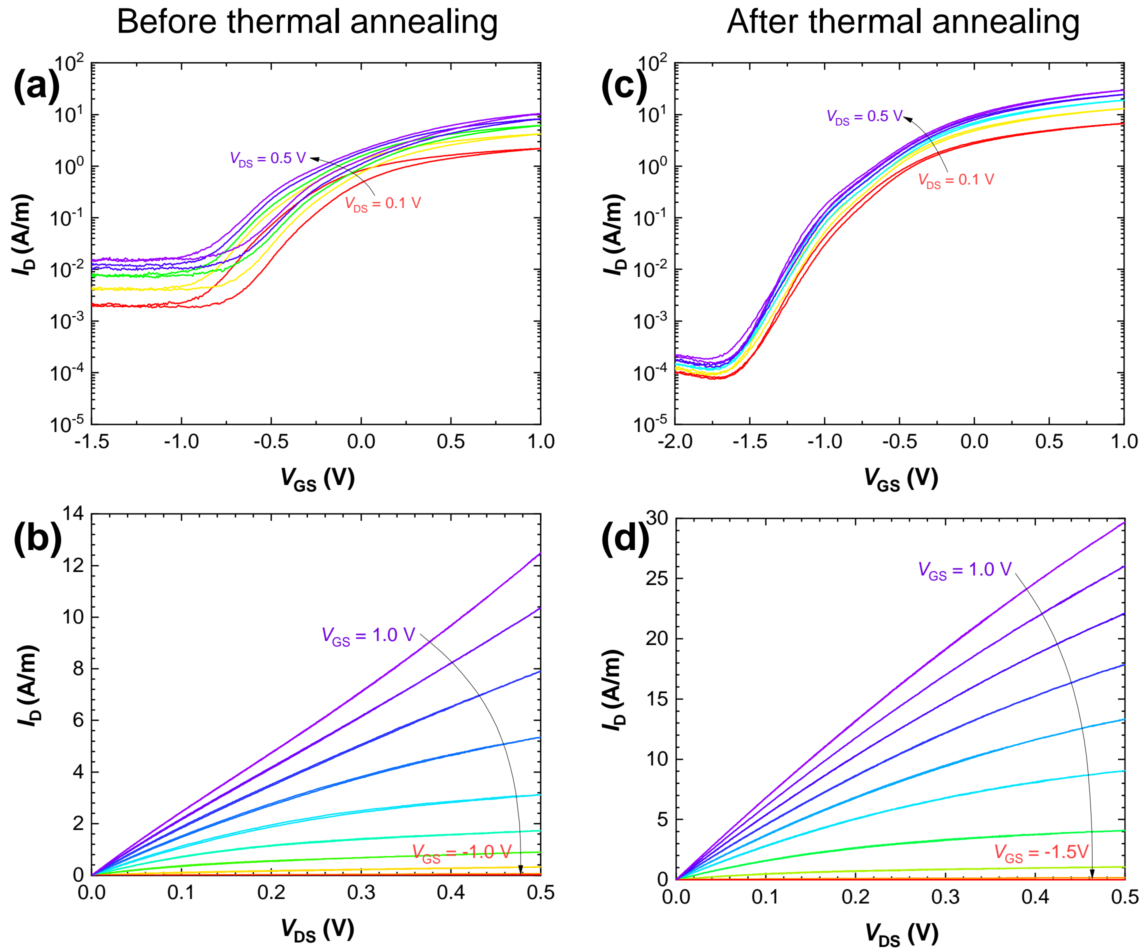

Figure S6. The influence of thermal annealing on the transistor properties of ultra-scaled MoS_2 FETs. (a) The transfer curves of a FET before annealing. (b) The output curves of the same FET before annealing. (a) The transfer curves of the same FET after annealing. (a) The output curves of the same FET after annealing.

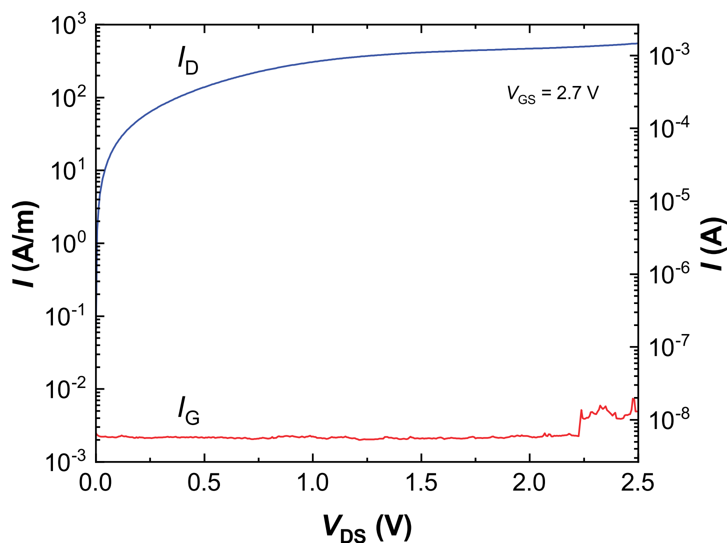

Figure S7. Drain (blue) and gate (red) currents corresponding to the highest drain current shown in Fig. 2(d) in the main text. The onset of the (reversible) gate oxide breakdown can be observed in the gate current for $V_{DS} > 2.25$ V due to a very large gate bias ($V_{GS} = 2.7$ V). However, the gate current is still ~ 5 orders of magnitude smaller than the drain current in this regime. The gate oxide irreversibly breaks at ~ 2.9 V.

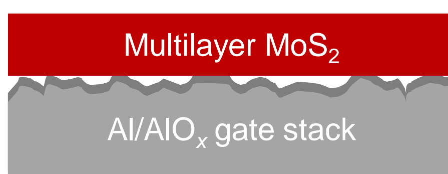

Figure S8. A multilayer MoS_2 flake smoothens out the roughness of the gate allowing a 10-nm separation between the source and drain contacts fabricated on top of the flake.

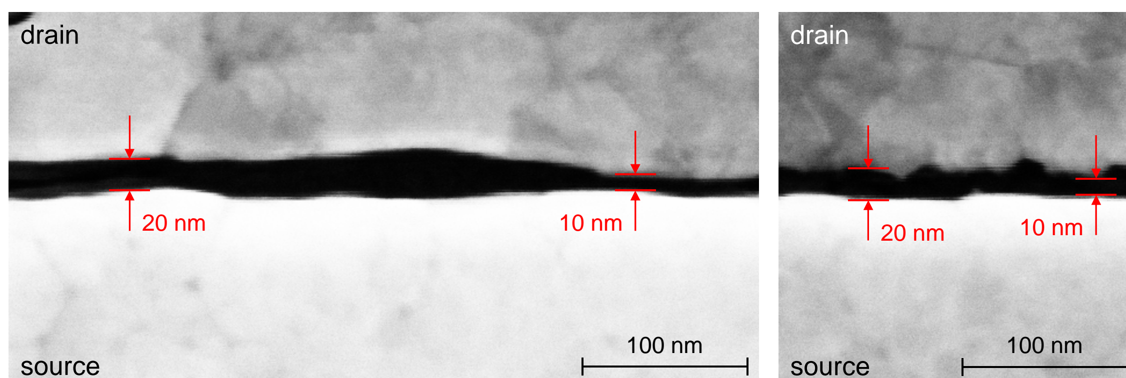

Figure S9. SEM images of gaps between source and drain contacts in two different CVD monolayer MoS_2 FETs.

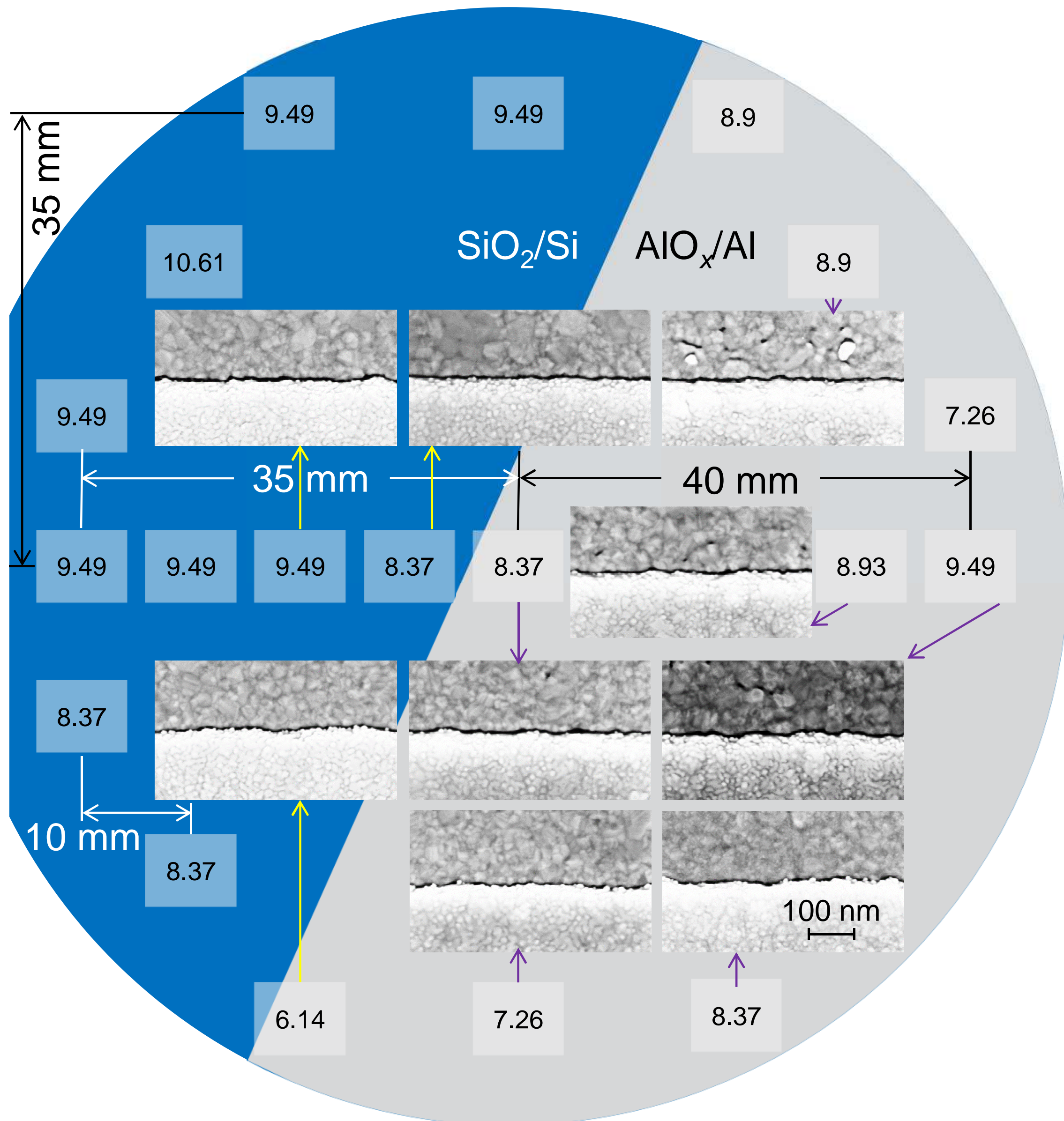

Figure S10. Ultra-scaled FETs fabricated on a 100 mm wafer. On one part (blue) of the wafer, the FETs were fabricated directly on the SiO_2/Si substrate, while on the other part (gray) they were fabricated on the Al/AlO_x gate. The numbers in bright rectangles indicate the gate length in nm (the length of the gap between the source and drain) at the location of the rectangles. The SEM images show the gap for some of the selected locations on the wafer. All SEM images are in the same scale, which is given in the bottom right image. Some distances on the wafer are also marked. The gap size uniformity is better on SiO_2/Si due to smaller surface roughness.

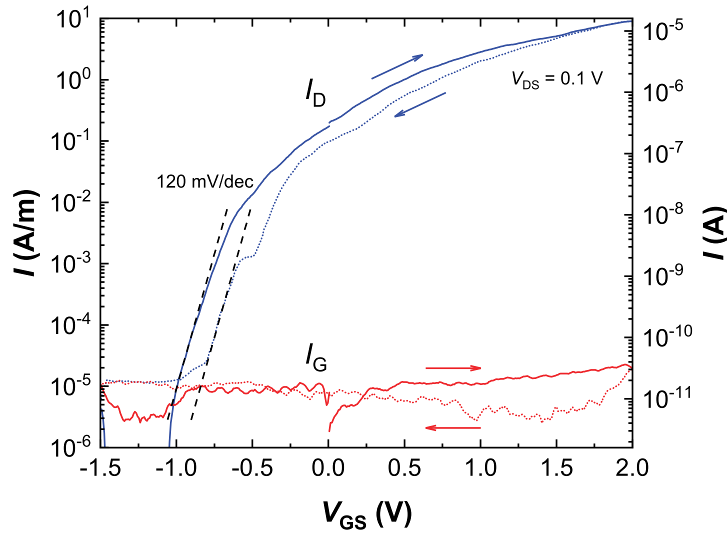

Figure S11. Drain (blue) and gate (red) currents in the subthreshold regime of the CVD MoS_2 FET shown in Fig. 3 in the main text. Both up (solid line) and down (dotted line) sweeps are shown (the sweep directions are also indicated by the arrows). The same subthreshold swing $S_{\mathrm{th}} = 120$ mV/dec was obtained both in the up and down sweep. The drain current I_{D} exhibits the obtained subthreshold swing in the range from $2.4 \cdot 10^{-5}$ to $4.5 \cdot 10^{-4}$ A/m (down sweep) and from $6 \cdot 10^{-6}$ to 10^{-4} A/m (up sweep). At the same time, the gate current is almost constant (down sweep) or exhibits ~ 24 times smaller change at ~ 480 mV/dec (up sweep). This indicates that the gate leakage current does not have an influence on the subthreshold regime of the FET. However, the drain current is almost constant for $V_{\mathrm{GS}} < -1$ V (down sweep) due to the influence of the gate leakage current.

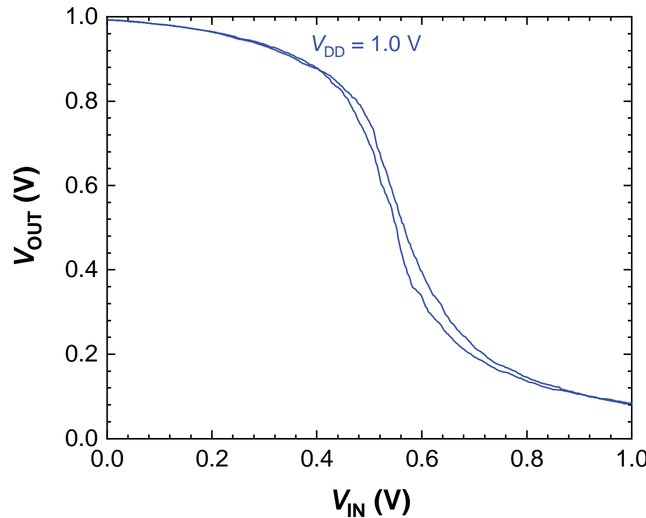

Figure S12. Static voltage transfer characteristic of a 10-nm inverter in a depletion-load technology on which the digital waveforms shown in Fig. 4(c) were measured.

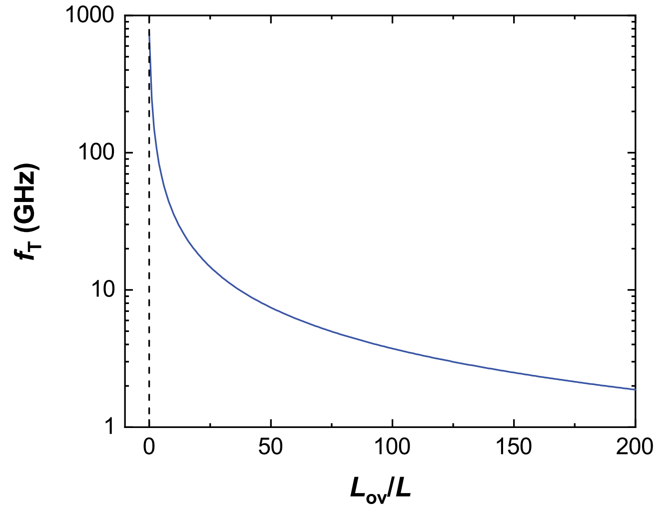

Figure S13. The extrinsic cutoff frequency f_T of a 10-nm MoS_2 FET as a function of the ratio between the overlap length L_{ov} and gate length $L = 10$ nm. The overlap length is the length of the gate below one of the contacts (source or drain). The total device capacitance is therefore $C = C_{ox}W(L + 2L_{ov})$, where $C_{ox} = 1.4$ μF/cm^2 [3, 4]. This gives for the cutoff frequency $f_T = g_m/(2\pi C) = (g_m/W2\pi C_{ox}L)/(1 + 2L_{ov}/L)$. For $g_m/W = 662$ S/m (as in the main text) and $L = 10$ nm, this leads to $f_T = 752$ GHz$/(1 + 2L_{ov}/L)$, i.e., $f_T = 752$ GHz for $L_{ov} = 0$ nm (no overlap) and 3.7 GHz for realistic $L_{ov} = 1$ μm. The reason for a large discrepancy between f_T and the clock rate of 2 kHz in Fig. 4(c) is due to different biasing. The cutoff frequency is measured in a single transistor circuit in which an FET is biased to be as highly conductive as possible (i.e., to operate at the highest possible drain current). However, the load FET in the inverter in Fig. 4 has $V_{GS} = 0$ V which cannot be changed due to the circuit layout. As n-type MoS_2 FETs do not conduct very well at $V_{GS} = 0$ V, the load FET behaves as a very large resistor which limits the bandwidth of the circuit. It would be necessary to operate the load FET with $V_{GS} \sim 2.5$ V (as in Fig. 2(d)) to get the high clock rate of the inverter.

References

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