Current saturation in zero-bandgap, top-gated graphene field-effect transistors

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Supplementary Information

Importance of front-gated device structures

Front-gated device structures are essential to provide the electrostatics required for exploring high-bias operation of graphene field-effect transistors. The geometry of back-gated GFET structures is constrained by the requirement that graphene be visible; as a result, most GFET devices are built with a thick (~ 300 nm) silicon dioxide dielectric layer. Figs. S1a-b below show the I-V characteristics of two back-gated GFET structures of widths 5.5 μm and 300 nm and lengths 3 μm and 150 nm, respectively. The long channel device in Fig. S1a shows a weak "kink" effect for V_{ds} values around 1.5 – 2.0 V. The effect is much less pronounced than for the top-gated device structures (Fig. 3) because of the inferior electrostatics coupling to the gate electrodes in the back-gated device; we believe that out-of-plane fringing fields from the drain have a significant "gating" influence on the graphene channel as electric field lines from the drain contact terminate in the graphene channel. This reaches an extreme for short-channel-length devices at high values of V_{ds}. As shown in Fig. S1b, the drain current shows a sharp increase, very similar to "punch-through" characteristics seen in short-channel-affected Si MOSFETs as the gate loses all control of conduction in the channel. At sufficiently high V_{ds}, this "runaway" drain current leads to irreversible thermal damage to graphene channels.

Fabrication details

The single-layer character of the sheets used for device fabrication are verified with Raman spectroscopy[1]. Fig. S2a shows the optical image of single-layer graphene and Fig. S2b shows the Raman spectroscopy results. Raman spectroscopy is performed after the HfO_2 gate dielectric deposition but prior to gate metal deposition. A weak D band peak at 1340 cm^{-1}, a G band peak

at 1583 cm^{-1}, and a sharp 2D band peak at 2682 cm^{-1} with a FWHM of 26 cm^{-1}indicates that the sample is single layer with few defects.

HfO_2 gate dielectrics are deposited with atomic layer deposition (ALD) in a Cambridge Nanotech ALD system with a tetrakis(dimethylamido)hafnium(IV) (Sigma Aldrich) precursor. The growth was carried out at 90 °C with a 0.3 sec pulse time for the hafnium precursor, followed by a 50 sec purge time, 0.03 sec H_2O pulse, and 150 sec purge time. The resulting growth rate is approximately 1 A°/cycle. The film thickness varies less than 2% across a 4" wafer and the dielectric constant is approximately 16 as determined by capacitance versus voltage (CV) measurements. The leakage current through the oxide is recorded throughout all device measurements and is below the detection limit of our measurement setup (<1 pA).

Figure S3 shows an atomic-force microscope (AFM) image of single layer graphene on SiO_2 with 5nm of HfO_2 grown directly after mechanical exfoliation. We can still measure the height of the graphene sheet (~9 A°) and find it to be consistent with the previous measurements[2,3], suggesting that the growth is taking place at the same rate both on the SiO_2 surface and on the graphene. As the graphene lattice does not have any dangling bonds on the surface, the growth is most likely due to physiosorption, which is enhanced by the low-temperature growth procedure. Alternatively, growth may also nucleate from ambient spices (e.g. water molecules or contaminants)adhering to the graphene surface. The roughness of the oxide on top of the graphene is observed to be ~30% higher than on the SiO_2, supporting the postulated growth mechanisms.

In order to determine the effect of the HfO_2 growth on the electronic properties of the graphene sheet, we measure I_d at $V_{sd} = 10\ mV$ as a function of $V_{gs\text{-}back}$ before and after the HfO_2 growth. Representative curves for one sample with width of 1.5 μm and length of 3 μm are shown in Fig. S4. While there is a small shift in the Dirac point, the mobility of the graphene sheet is largely the same before and after HfO_2 growth.

Room-temperature small-signal characterization

Fig. S5 shows the same low-field transport characterization of Fig. 1e at room temperature. In this case, the hysteresis hinders the extraction of the C_{top}/C_{back} capacitance ratio. We attribute the hysteresis to trapped charges between graphene and the HfO_2 and inside the HfO_2 that freeze out at low temperatures. We perform the room-temperature I-V measurements of Figs. 2-4 with consistent $V_{gs\text{-}top}$ sweep directions, allowing reproducibility of these measurements despite the effects of trapped charge.

Graphene FET model

An analytic expression for the drain current can be derived, including velocity saturation effects. The current in the channel is given by:

$$I_d = \frac{W}{L}\int_0^L en(x)v_{drift}(x)dx$$

Where L is the channel length and W is the channel width. Using the expressions for $n(x)$ and $v_{drift}(x)$ provided in the Letter, we find:

$$I_d = \frac{\frac{W}{L} e\mu \int_{R_s I_d}^{V_{gd}-R_s I_d} \sqrt{n_0^2 + \left(C_{top}\left(V_{gs-top} - V - V_0\right)/e\right)^2}\, dV}{1 + \frac{\mu(V_{sd} - 2R_s I_d)}{L v_{sat}}}$$

where R_s is the source-drain series resistance. This can be integrated and the resulting transcendental equation solved numerically.

Velocity saturation

We assume a model in which velocity saturation is caused by scattering from phonons in which the coupling to the phonon is strong enough that once the electron reaches the energy threshold for phonon emission, it is immediately scattered. This means that the Fermi sea will be shifted by the phonon energy $\hbar\Omega$. The current density carried by such a shifted sea in the direction of the applied electric field is given by:

$$j = e \int \frac{d\boldsymbol{k}}{\pi^2} v_F \cos^2\theta\, \hbar\Omega \left(-\frac{\partial f}{\partial E}\right)\Big|_{E=\hbar v_F k}$$

where θ is the angle between $d\boldsymbol{k}$ and the electric field and f is the Fermi-Dirac distribution function. Writing the integral in polar coordinates,

$$j = e \int_0^{\infty} \frac{dk}{\pi^2} k \int_0^{2\pi} d\theta\, v_F \cos^2\theta \hbar\Omega \delta(\hbar v_F k - E_F)$$

$$= \frac{e}{\pi} \Omega \frac{E_F}{\hbar v_F}$$

Taking the current density to be $j = nev_{sat}$, with $E_F = \hbar v_F \sqrt{\pi n}$ yields :

$$v_{sat} = v_F \frac{\hbar\Omega}{E_F}$$

This result implies that v_{sat} is concentration-dependent for graphene; the higher the concentration, the lower the v_{sat}. While semiconductors have v_{sat} values limited by the thermal velocity[4], v_{sat}values for graphene are instead limited by v_F. It is important to note that this derivation assumes that this expression is not valid in the vicinity of the Dirac point.

Supplementary References

[1] Ferrari, A. C. *et al.*, Raman Spectrum of Graphene and Graphene Layers. *Phys. Rev. Lett.* **97,** 187401-187404 (2006).

[2] Novoselov, K. S. *et al.*, Electric Field Effect in Atomically Thin Carbon Films. *Science* **306** (2004).

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Supplementary Figure Captions

Figure S1. **I-V characteristics of back gated GFETs.** I-V characteristics of back-gated GFET with a 300 nm-thick oxide. **a,** Device width is 5.5 μm and length is 3 μm for $V_{gs\text{-}back}$*= 1 V* to $V_{gs\text{-}back}$*= 9 V* in *2 V* steps. **b,** Short-channel device with width 300 nm and length 150 nm showing "punch-through" behavior for $V_{gs\text{-}back}$*= 14 V* to $V_{gs\text{-}back}$*= 17 V* in *1 V* steps.

Figure S2. **Characterization of mechanically exfoliated graphene sheets. a,** Graphene sheets can be optically discriminated on 300 nm SiO_2 oxides on Si wafers. **b**, Raman spectroscopy is used to verify the single-layer characteristics of the graphene sheets after device fabrication. The sharp 2D peak at 2682 cm^{-1} shows clearly the single layer characteristics of the graphene piece. The weak D band at 1340 cm^{-1} indicates that the sample has view defects.

Figure S3. **Atomic-force microscopy (AFM) image of graphene covered with HfO_2.** Graphene sheet covered with 5 nm HfO_2 prior to fabrication of any contacts. The thickness of the piece is 9 A° suggesting that the growth takes place at the same rate on both SiO_2 and graphene.

Figure S4. **I_d as a function of $V_{gs\text{-}back}$ at V_{sd} = 10 mV for a GFET device with width of 1.5 μm and length of 3 μm.** The mobility before and after HfO_2 growth is largely unchanged.

Figure S5. **Room temperature low-field transport in front-gated GFET**. g_{ds} as a function of $V_{gs\text{-}top}$ at $V_{gs\text{-}back}$ *= -40 V* for both sweep directions. A hysteresis of 1.26 V can be observed due to trapped charges.

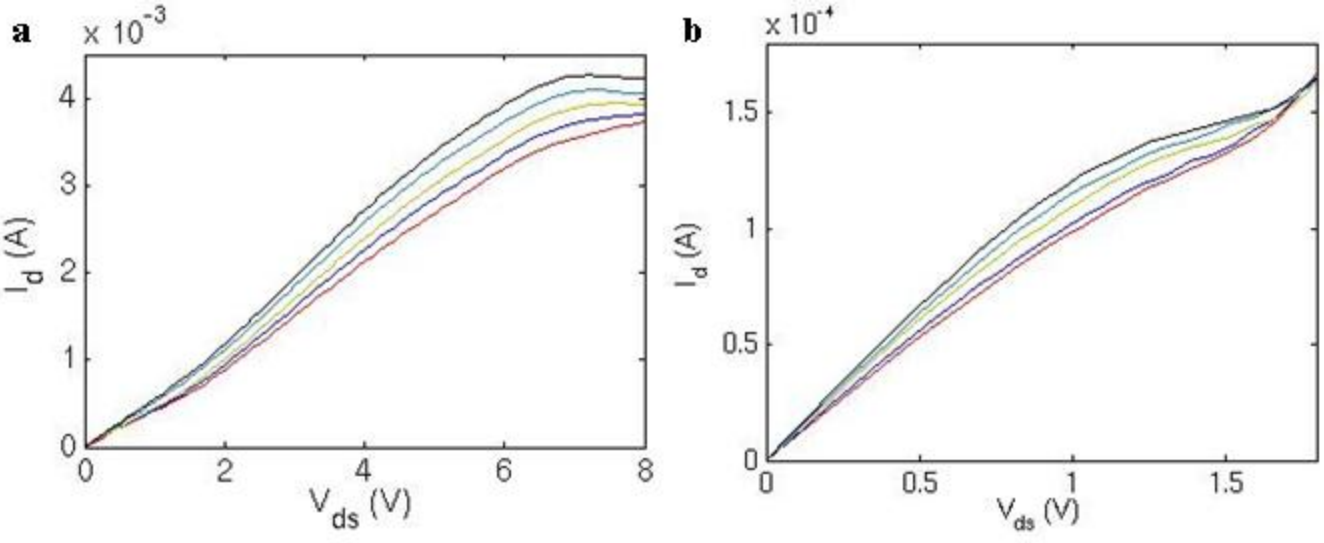

Figure S1. **I-V characteristics of back gated GFETs.**

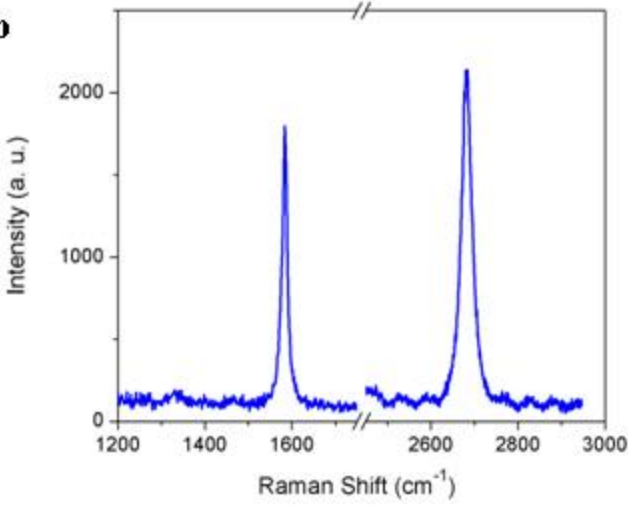

Figure S2. **Characterization of mechanically exfoliated graphene sheets.**

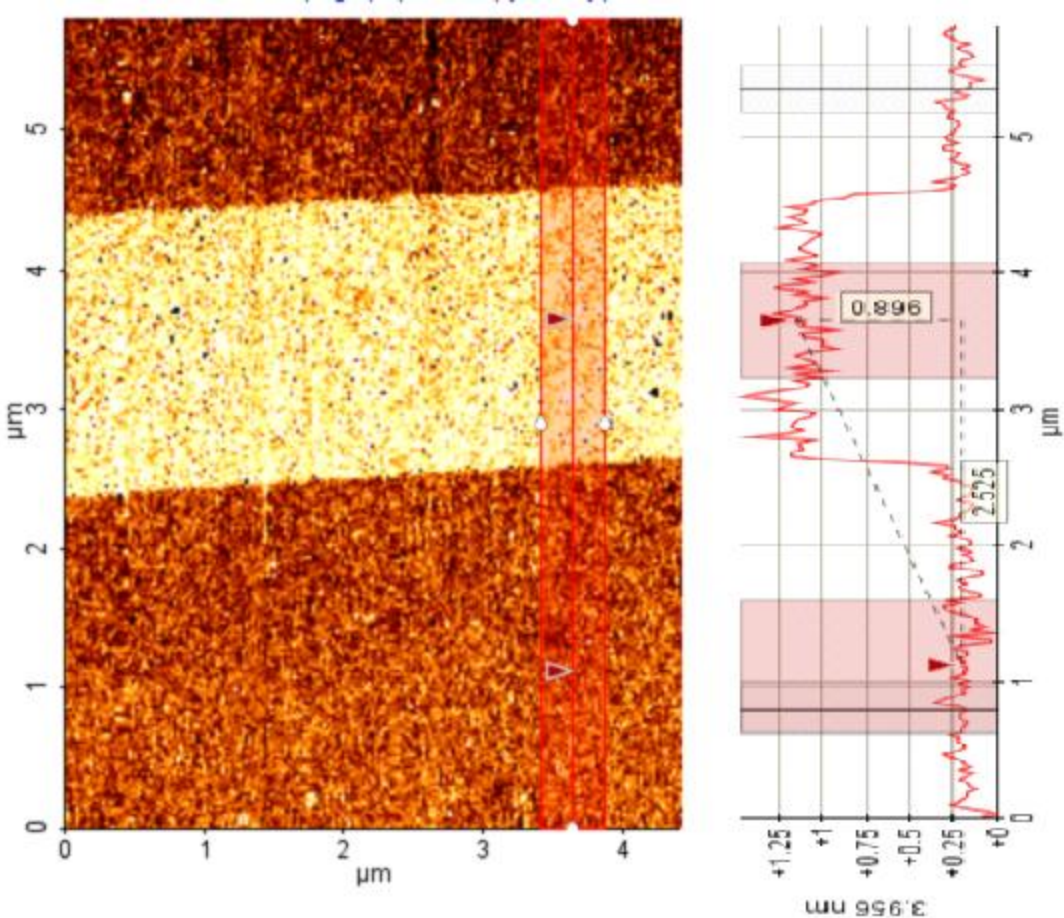

Figure S3. **Atomic-force microscopy (AFM) image of graphene covered with HfO_2.**

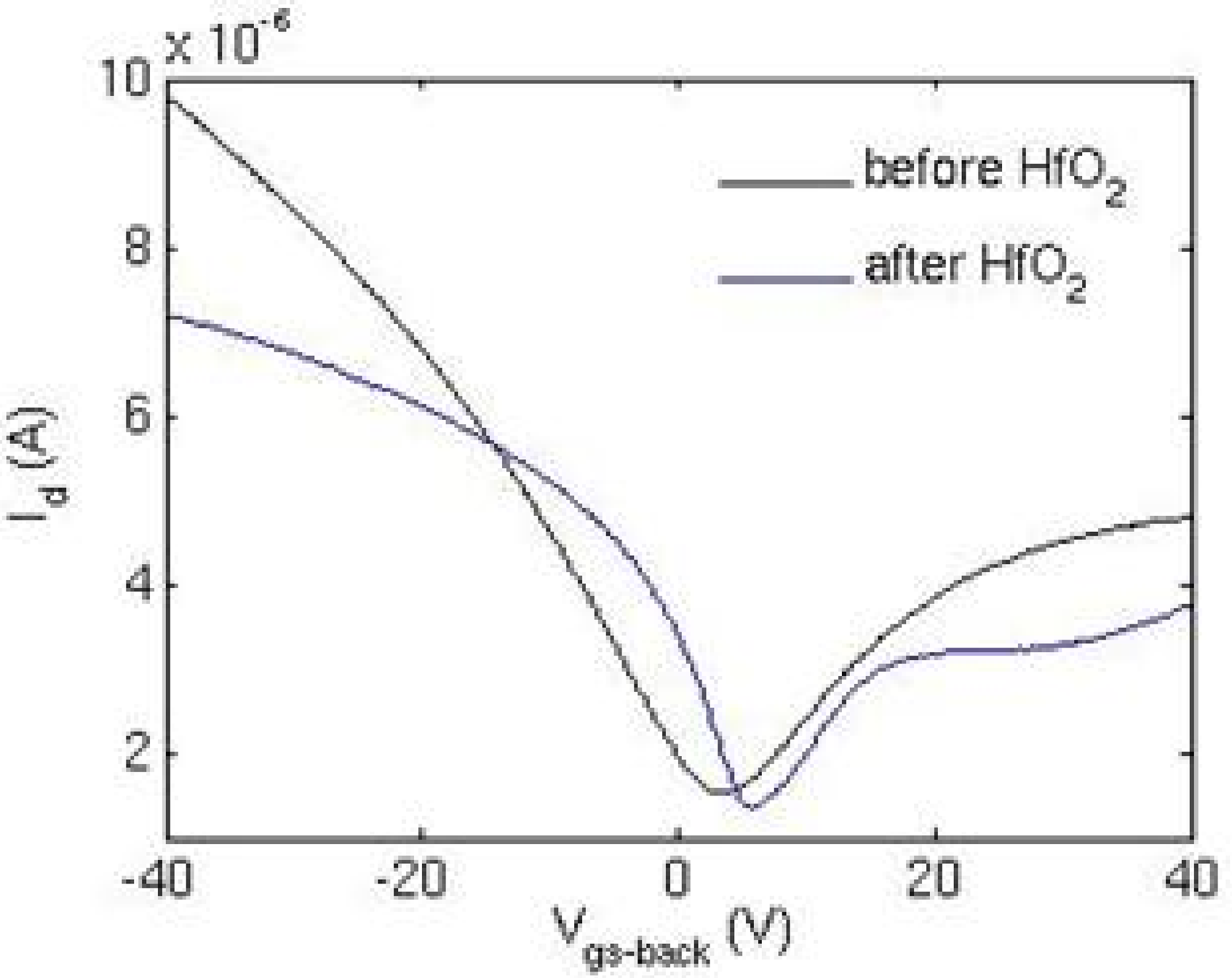

Figure S4. **I_d as a function of $V_{gs\text{-}back}$ for V_{ds} = 10 mV for a GFET device with width of 1.5 µm and length of 3 µm.**

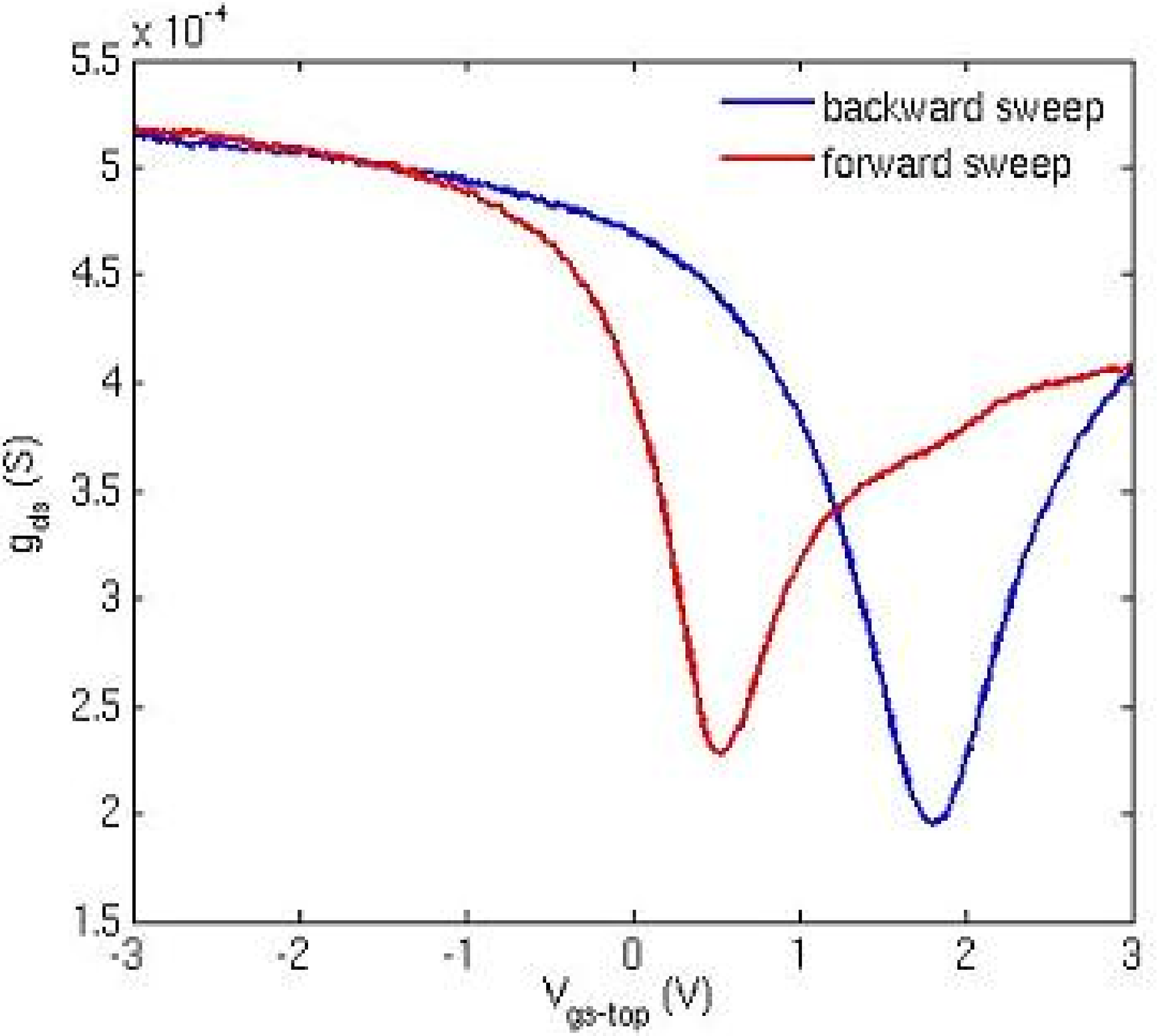

Figure S5. **Room temperature low-field transport in front-gated GFET**